ROLL NO. _____

Code: AE74 **Subject: VLSI DESIGN**

AMIETE – ET

Time: 3 Hours **JUNE 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The material used for developing insulating layer between gate and substrate is

(A) Polysilicon **(B)** Silicon dioxide
(C) Boron **(D)** Arson

b. The polarity of NMOS depletion type FET gate voltage is

(A) Positive **(B)** Negative
(C) Neutral **(D)** Both positive & negative

c. The circular disc used for IC fabrication is named as

(A) Cylinder **(B)** Plate
(C) Wafer **(D)** CD

d. The nominal threshold voltage for NMOS enhancement type MOSFET is

(A) 0.3 VDD **(B)** 0.1 VDD
(C) 0.4 VDD **(D)** 0.2 VDD

e. Typical values of μ at room temperature are

(A) $\mu_n = 650\text{cm}^2/\text{V sec}$, $\mu_p = 240\text{cm}^2/\text{V sec}$
(B) $\mu_n = 65\text{cm}^2/\text{V sec}$, $\mu_p = 24\text{cm}^2/\text{V sec}$
(C) $\mu_n = 1250\text{cm}^2/\text{V sec}$, $\mu_p = 480\text{cm}^2/\text{V sec}$
(D) $\mu_n = 125\text{cm}^2/\text{V sec}$, $\mu_p = 480\text{cm}^2/\text{V sec}$

f. In BiCMOS Inverters, the design approach is to use

(A) MOS - Logic
BIPOLAR – Driving
(B) MOS – Logic & Driving
BIPOLAR - Switching
(C) MOS - Driving
BIPOLAR – Logic
(D) None of these

g. Latch-up problem is negligible in _____fabrication method

(A) Twin tub process
(B) N-Well Process
(C) P-Well Process
(D) None of these

h. NMOS pass transistor has_____ voltage level degradation

(A) Low level
(B) High level
(C) Both **(A)** & **(B)**
(D) None of these

i. R_{on} of NMOS Z_{pu} / Z_{pd} ratio of 8:1 is _____ (Assume 5 micron technology)

(A) 40 KΩ
(B) 50 KΩ
(C) 60 KΩ
(D) 90 KΩ

j. Optimization in Area, speed and power can be achieved in _____ design style

(A) Full custom
(B) Semi custom
(C) ASIC
(D) Gate array

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Write the basic structure of NMOS transistor for enhancement and depletion mode indicating all layers. **(4)**

b. With neat sketch explain the NMOS n-well Fabrication process. **(8)**

c. Compare CMOS technology with Bipolar technology. **(4)**

Q.3 a. Derive an expression for I_{ds} in terms of K, $\left(W/L\right)$ ratio and V_{ds} in both saturation and non – saturation. **(8)**

b. With neat circuit diagrams explain the various form of pull up used in MOS circuits. Compare the merits and demerits of each. **(8)**

Q.4 a. Write the circuit and stick diagram for
(i) two input CMOS NAND gate
(ii) y = AB+CD **(8)**

b. Write the design rules of transistor, wires and contacts. Explain briefly with neat sketch **(8)**

Q.5 a. Determine the total delay of NMOS and CMOS inverter pair. **(4)**

b. Calculate the capacitance of a metal layer with L = 20 λ and width = 3λ in terms of standard unit of capacitance. **(4)**

c. Derive an expression for total delay of N inverters (NfMOS) connected in cascaded form to drive a large capacitive load. **(8)**

Q.6 a. Explain briefly three different scaling models defined in VLSI design. **(6)**

b. Draw schematic and stick diagram of an 2-input NOR-gate using CMOS and BiCMOS logic. **(10)**

Q.7 a. Design an adder element that can be cascaded to form 'n' bit adder. **(6)**

b. Write the circuit of Manchester carry chain element. Explain briefly with figure the requirement of buffering in cascaded Manchester carry chain circuit. **(10)**

Q.8 a. Write the circuit of three transistor dynamic RAM cell and explain briefly read and write functions. **(10)**

b. Write note on factors influencing choice of layer for wiring. **(6)**

Q.9 a. With an example explain sensitized path based testing used for combination logic circuit. **(8)**

b. Explain DRC, Circuit Extractor and Simulator with example. **(8)**