ROLL NO. _____

Code: AE54/AC54/AT54 Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT

JUNE 2013

Time: 3 Hours **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. An Op-amp act as a voltage follower has a voltage gain of

(A) Infinity **(B)** Zero
(C) Unity **(D)** Less than unity

b. A bistable multivibrator is a

(A) Free running oscillator **(B)** Triggered oscillator
(C) Saw tooth wave generator **(D)** Crystal oscillator

c. A virtual ground

(A) is a ground for voltage
(B) is a ground for both voltage and current
(C) is ground for current
(D) is a ground for voltage but not for current

d. An ideal differential amplifier has CMRR equaling

(A) Unity **(B)** – 1 (minus unity)
(C) Infinity **(D)** Zero

e. When a sinusoidal voltage wave is fed to a Schmitt trigger, the output will be

(A) triangular wave **(B)** square wave
(C) d.c. **(D)** trapezoidal wave

f. The large signal bandwidth of an opamp is limited by its

(A) Loop gain **(B)** slew rate
(C) output impedance **(D)** input frequency

g. A 'literal' in Boolean Algebra means

(A) a variable in its uncomplemented form only
(B) a variable ORed with its complement
(C) a variable in its complemented form only
(D) a variable in its complemented or uncomplemented form

h. Simplified expression of $xy + xyz + \bar{x}y + x\bar{y}z$ is

(A) $\bar{y} + x\bar{z}$ **(B)** $\bar{x} + \bar{y}z$
(C) $y + xz$ **(D)** $y + \bar{x}z$

i. In an SR flip flop S = 1 and R = 1 gives

(A) Set state **(B)** Reset state
(C) Indeterminate state **(D)** None of these

j. The logic gate which detects equality of two bits is

(A) EX-OR **(B)** Ex-NOR
(C) NOR **(D)** NAND

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

Q.2 a. Classify ICs on the basis of applications, devices used and chip complexity. **(8)**

b. In the differential amplifier circuit shown below, the transistors have identical characteristics and their β =100. Determine the **(8)**
(i) output voltage
(ii) the base currents and
(iii) the base voltages taking into account the effect of the R_B and V_{BE}.
Assume V_{BE}=0.7 Volts, $R_B = 25K\Omega$, $R_C = 12K\Omega$ and $R_E = 8K\Omega$.
$V_{EE} = -12V$, $V_{CC} = +12V$

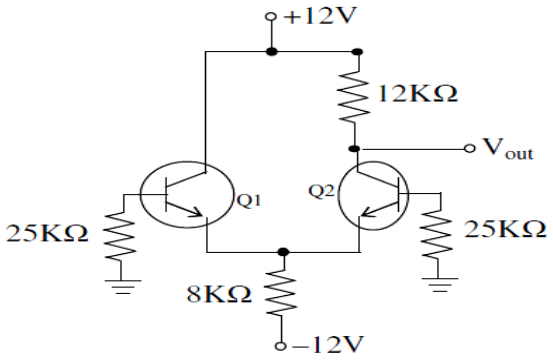

Fig.1

Q.3 a. Explain what you understand by 'offset voltage' and 'offset current' of op-amp. Discuss with a neat circuit diagram the technique used for minimizing offset voltage and offset current in an inverting amplifier. **(10)**

b. Calculate the output voltage 'V_0' for the following non-inverting op-amp summer with V_1 =2V and V_2 = -1V **(6)**

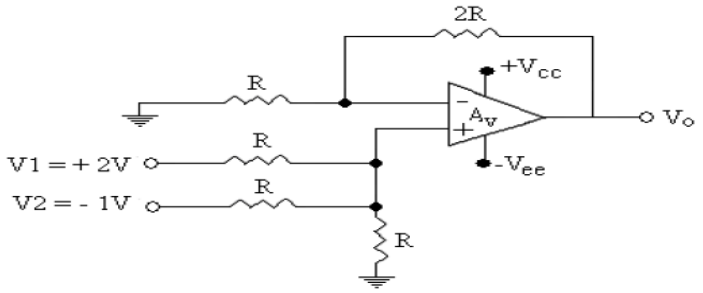

Fig.2

Q.4 a. Explain Schmitt trigger with the help of transfer characteristics. Also obtain the expression of hysteresis voltage V_H and output waveform for sinusoidal input signal. **(8)**

b. The input to an op-amp differentiator circuit is a sinusoidal voltage of peak value 10μV and frequency of 2 kHz. If the values of differentiating components are given as R = 40 kΩ and C =3μF, determine the output voltage of differentiator circuit. **(8)**

Q.5 a. Explain the working of R-2R Ladder Digital to Analog Converter. **(6)**

b. Explain Monostable multivibrator circuit operation using 555 timers. Also, determine the frequency of output signal. **(6)**

c. Explain the working of Series Op-Amp Regulator. **(4)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 a. Differentiate between analog and digital signals. **(4)**

b. Explain the concept of Parity bits with reference to error detection. **(6)**

c. Convert the following: **(6)**
(i) $(5A34F)_{16}$ to binary
(ii) $(56)_{10}$ to Gray Code
(iii) $(93)_{10}$ to Excess-3 Code

Q.7 a. Simplify the Boolean function 'F' together with don't care conditions 'd' in sum of Products
$F(w, x, y, z) = \sum(0,1,2,3,7,8,10)$
$d(w, x, y, z) = \sum(5,6,11,15)$ **(6)**

b. State and prove De Morgan's theorem using truth table. **(6)**

c. Show that NAND gate is a Universal gate. **(4)**

Q.8 a. Explain the 4-bit parallel binary adder. **(8)**

b. Write a short note on 8: 1 Multiplexers. **(8)**

Q.9 a. Draw and explain the working of NAND-gate latch. **(6)**

b. Distinguish between synchronous and asynchronous counters. Design a 3-bit UP-DOWN synchronous counter. **(10)**