ROLL NO. _____

Code: AC58/AT58 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT

Time: 3 Hours **JUNE 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. A logic circuit that can add two binary numbers is _____.

(A) OR **(B)** AND
(C) NAND **(D)** NOT

b. When a subroutine is called, the address of the instruction following the CALL instructions is stored in/on the

(A) stack pointer **(B)** accumulator
(C) program counter **(D)** stack

c. Memory access in RISC architecture is limited to instructions

(A) CALL and RET **(B)** PUSH and POP
(C) STA and LDA **(D)** MOV and JMP

d. The branch logic that provides decision making capabilities in the control unit is known as

(A) controlled transfer **(B)** conditional transfer
(C) unconditional transfer **(D)** none of these

e. Interrupts which are initiated by an instruction are

(A) internal **(B)** external
(C) hardware **(D)** software

f. Pipelining strategy is called implement

(A) instruction execution **(B)** instruction prefetch
(C) instruction decoding **(D)** instruction manipulation

g. How many address lines are needed to address each memory locations in a 2048 X 4 memory chip?

(A) 10 **(B)** 11
(C) 8 **(D)** 12

h. When the RET instruction at the end of subroutine is executed,

(A) The information where the stack is initialized is transferred to the stack pointer
(B) The memory address of the RET instruction is transferred to the program counter
(C) Two data bytes stored in the top two locations of the stack are transferred to the program counter
(D) Two data bytes stored in the top two locations of the stack are transferred to the stack pointer

i. The method for updating the main memory as soon as a word is removed from the Cache is called

(A) write-through **(B)** write-back
(C) protected write **(D)** cache-write

j. How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(A) 8 **(B)** 16
(C) 24 **(D)** 32

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Define processor clock and clock rate. **(4)**

b. Explain instruction sequencing and give an illustration. **(3+3)**

c. Explain input, output and arithmetic logic unit of a computer. **(6)**

Q.3 a. Explain how stack is used for nested subroutines. Show the flow of execution using a suitable example. **(10)**

b. Explain Autoincrement and Autodecrement mode. Where are these used? **(6)**

Q.4 a. Describe the hardware mechanism for handling multiple interrupt requests. **(4)**

b. What are handshaking signals? Explain the handshake control of data transfer during input and output operation. **(6)**

c. Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals. **(6)**

Q.5 a. What are the needs for input-output interface? Explain the functions of a typical 8-bit parallel interface in detail. **(8)**

b. Describe the USB architecture with the help of a neat diagram. **(8)**

Q.6 a. Explain the cache with two-way set-associative addressing. Give an illustration. **(6)**

b. Briefly explain asynchronous and synchronous DRAMs. **(10)**

Q.7 a. Design a fast adder. What are the variations in a fast adder? **(6)**

b. Explain how the virtual address is converted into real address in a paged virtual memory system. Give an example. **(8)**

c. Differentiate between magnetic-disk and CD-ROM systems. **(2)**

Q.8 a. Give the algorithm for multiplication of signed 2's complement numbers and illustrate with an example. **(8)**

b. Explain the representation of floating point numbers in detail. Give the IEEE standard double precision floating point format. **(8)**

Q.9 a. What are the advantages and disadvantages of hardwired and microprogrammed control? **(5)**

b. Draw neat diagram of single bus organization of CPU showing ALU, all types of registers and the data paths among them. Compare it with multiple bus organization of CPU. **(11)**