ROLL NO. _____

Code: DE58/DC58/DE108/DC108 **Subject: LOGIC DESIGN**

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **JUNE 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The Gray code for binary number 1101 is equivalent to

(A) 1101 **(B)** 1011
(C) 0101 **(D)** 1110

b. Output is high, when all input variables are high than logic gate is

(A) AND **(B)** OR
(C) NOT **(D)** EX-OR

c. Result of adding $(01101)_B$ with $(01111)_B$ is

(A) 11010 **(B)** 10110
(C) 11110 **(D)** 11100

d. A decoder with 3 inputs can have a maximum of _____ unique outputs.

(A) 6 **(B)** 7
(C) 8 **(D)** 4

e. Which of the following is a sequential circuit:

(A) decoder **(B)** multiplexer
(C) counter **(D)** encoder

f. Master slave JK flip flop is used to avoid the following problem

(A) noise **(B)** delay
(C) thermal run away **(D)** race - around problem

g. A four bit synchronous counter is constructed using JK flip flop. The JK flip flop has propagation delay of 24 ns, the maximum frequency that can be used is given by

(A) 10.4 MHz **(B)** 12.4 MHz
(C) 14.4 MHz **(D)** 16.4 MHz

h. How many Flip-Flops are required for mod–16 counter?

(A) 16 **(B)** 12
(C) 8 **(D)** 4

i. The gates required to build a half adder are

(A) XOR gate and NOR gate **(B)** XNOR gate and NOR gate
(C) XOR gate and AND gate **(D)** XOR gate and NOT gate

j. How many address lines are required to access 4K Byte memory?

(A) 10 **(B)** 12
(C) 8 **(D)** 16

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Perform the following conversions: **(8)**

(i) $(735)_8 = (?)_2$

(ii) $(37FD)_{16} = (?)_{10}$

(iii) $(37.45)_{10} = (?)_2$

(iv) BCD number 1001001110000110 in to its decimal equivalent.

b. Define binary system. **(2)**

c. What are advantages and limitations of digital system over analog system? **(6)**

Q.3 a. What do you mean by universal gate? Implement AND, OR and NOT gate using any one of universal gate. **(5)**

b. Simplify the following expression, construct the corresponding logic circuit using basic gates. **(6)**

$Y = A + \overline{B}C + ABC + A\overline{B}C$

c. Draw the symbol of XNOR gate and explain its working with the help of truth table. **(5)**

Q.4 a. Perform the following operations: **(8)**
(i) Subtract -36 from - 15 using 2's complement.
(ii) Add 623 and 599 using BCD code.

b. Design and explain full adder circuit using truth table. **(8)**

Q.5 a. Draw the circuit of 4 bit serial in serial out shift register and explain its working. **(8)**

b. Explain design procedure to design synchronous counter whose state transition diagram is shown in **Fig.1**. **(8)**

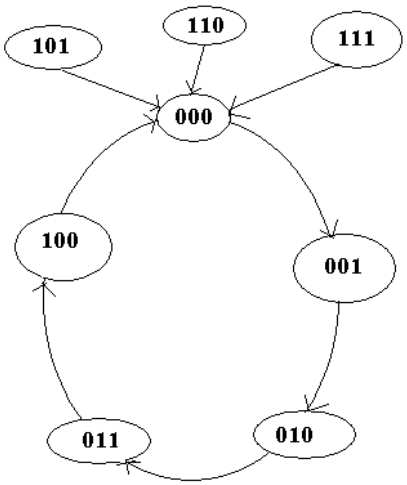

Fig.1

Q.6 a. What is decoder? Explain working of a 3 to 8 line decoder with the help of its detailed logic diagram and truth table. **(8)**

b. What is multiplexer? Draw logic diagram of four inputs multiplexer and explain its working. **(8)**

Q.7 a. Draw the logic diagram of JK flip flop and explain its working using truth table. **(6)**

b. Consider the circuit shown in **Fig.2**, **(10)**

(i) Determine the counter's MOD number

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(ii) Determine the frequency at the output of the last FF (Q2) when the input clock frequency is 1MHz.

(iii) What is the range of counting state for this counter?

(iv) Assume starting state is 000. What will be the counter's state after 129 pulses?

(v) Draw waveforms at Q_0, Q_1, and, Q_2 for the 10 input clock pulses.

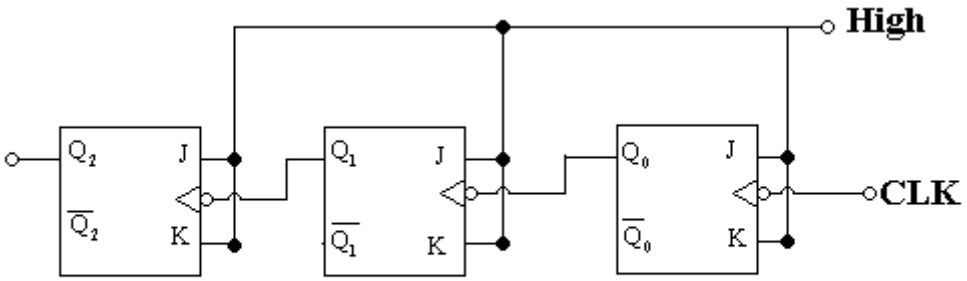

Fig.2

Q.8 a. Explain working principle of ripple counter with suitable logic diagram. **(8)**

b. Design a mod 8 synchronous up/down counter and explain its working with the help of timing wave form. **(8)**

Q.9 a. Explain with neat diagrams RAM architecture. **(8)**

b. Describe CPU – Memory connection with suitable block diagram. **(8)**