ROLL NO.

Code: DC57/DC107

Subject: COMPUTER ORGANIZATION

## **DiplETE – CS (Current & New Scheme)**

Time: 3 Hours

# **JUNE 2015**

Max. Marks: 100

 $(2 \times 10)$ 

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

#### NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

#### Q.1 Choose the correct or the best alternative in the following:

a. For a processor, length of one clock cycle is 2ms what is the clock rate.

(A) 200Hz	<b>(B)</b> 500Hz
(C) 500MHz	( <b>D</b> ) 50Hz

b. 2's complement addition of +4 and -6 is

( <b>A</b> ) 1101	<b>(B)</b> 1111
( <b>C</b> ) 1110	( <b>D</b> ) 1001

c. When I/O devices and the memory share the same address space, the arrangement is called

(A) Programmed-controlled I/O	( <b>B</b> ) I/O mapped I/O
(C) I/O mapped-memory	( <b>D</b> ) Memory-mapped I/O

d. The device that is allowed to initiate data transfers on the bus at any given time is called

(A) Bus master	<b>(B)</b> Bus slave
(C) Bus grant	<b>(D)</b> Bus arbiter

e. A serial port is used to connect the processor to I/O devices that require transmission of data

<b>(A)</b>	2 bits at a time	<b>(B)</b> 1 bit at a time
<b>(C)</b>	3 bits at a time	<b>(D)</b> Multiple bits at a time

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f.	Memories that consists of circuits capable of retaining their state as long as power is applied are known as		
	<ul><li>(A) Dynamic</li><li>(C) Non Static</li></ul>	<ul><li>(B) Static</li><li>(D) None of these</li></ul>	
g.	. Which is the fastest memory among the following		
	<ul><li>(A) Magnetic disk</li><li>(C) Registers</li></ul>	<ul><li>(B) Main memory</li><li>(D) Primary cache</li></ul>	
h.	h. The binary addresses that the processor issues for either instructions or data are called		
	<ul><li>(A) Virtual address</li><li>(C) Both (A) &amp; (B)</li></ul>	<ul><li>(B) Logical address</li><li>(D) None of these</li></ul>	
i.	Seek time		
	<ul> <li>(A) Time required to move the read/write head to proper track</li> <li>(B) Time required to move the read/write head to proper sector</li> <li>(C) Both (A) &amp; (B)</li> <li>(D) None of these</li> </ul>		
j.	In double precision floating bits	-point format mantissa fraction occupies how many	

( <b>A</b> ) 64	<b>(B)</b> 52
( <b>C</b> ) 23	<b>(D)</b> 8

### Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2	a.	Explain basic functional units of a computer with the help of neat blo diagram.	ck (8)
	b.	What is bus? Explain single bus structure with the help of neat diagram.	(8)
Q.3	a.	Explain how data transfer is achieved between memory of a computer and the outside world.	(10)
	b.	Define subroutine. Explain linking of subroutines using link register.	(6)
Q.4	a.	Explain the use of DMA controllers in a computer system.	(8)
	b.	Define Bus Arbitration. Explain centralised Arbitration.	2+6)

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Q.5	a.	Explain serial port with the help of serial interface block diagram.	(8)
	b.	Explain the use of PCI bus in a computer system.	(8)
Q.6	a.	Describe the working of static RAM cell.	(4)
	b.	Write the timing diagram for burst read of length 4.	(6)
	c.	Explain different types of read only memories.	(6)
Q.7	a.	Explain virtual-memory address translation without using TLB.	(8)
	b.	Explain 4-bit adder with carry look ahead logic.	(8)
Q.8	a.	Explain sequential circuit binary multiplier with an example.	(8)
	b.	Write the circuit arrangement for restoring division.	(4)
	c.	Write the algorithm for non restoring division.	(4)
Q.9	<b>)</b> a.	<ul><li>Write the control sequence for the following:</li><li>(i) Instruction add (R3), R4</li><li>(ii) Unconditional Branch Instruction</li></ul>	(5×2)
	b.	Write the three bus organization of the data path.	(6)