ROLL NO. _____

Code: CT12 **Subject: COMPUTER ARCHITECTURE**

ALCCS

Time: 3 Hours **JUNE 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Discuss about error detection and correction using parity checkers and generators.

b. Compare Horizontal Micro Code & Vertical Micro Code.

c. What is meant by overflow in binary addition and how is it detected?

d. Write short notes on Assemblers.

e. Name few high performance techniques to improve system performance.

f. Elaborate the concept of memory interleaving.

g. How do you explain the computer system from the following different views?
(i) Programmer's view
(ii) Computer architect's view **(7 × 4)**

Q.2 a. Discuss the following addressing modes with functional diagrams: **(9)**
(i) Register direct addressing
(ii) Relative addressing
(iii) Index addressing

b. What is the philosophy of RISC based machine? How is it different from a CISC Based machine? Discuss briefly. **(9)**

Q.3 a. Classify computers based on the instruction formats of CPU organization. Explain each with an example**.** **(9)**

b. Compare micro programmed control versus hardwired control. **(9)**

Q.4 a. Discuss about the special values and exceptions in floating point number system and obtain the range of numbers that can be represented using that format. **(9)**

b. Explain in detail about memory hierarchy. **(9)**

Q.5 a. Discuss associative mapping technique and state its advantages over direct mapping technique. **(9)**

b. A block set-associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks each consisting of 128 words.
(i) How many bits are there in the main memory address?
(ii) How many bits are there in each of TAG, SET, WORD fields? **(9)**

Q.6 a. Differentiate priority interrupt and daisy chain priority interrupt. **(9)**

b. Explain superscalar, super pipelined and VLIW architecture. **(9)**

Q.7 a. Perform addition and subtraction on the operands. The format is **(9)**

sign	Excess 15 exponent	Fractional mantissa
1 bit	5bits	6 bits

The operands are A =

0	10001	011011

The operands are B =

0	01111	101010

b. Differentiate parallel processing and pipeline processing. **(9)**