ROLL NO. _____

Code: AE74 **Subject: VLSI DESIGN**

AMIETE – ET (Current Scheme)

Time: 3 Hours **JUNE 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The deficiency of MOS technology is

(A) Low Density **(B)** Load Driving Capabilities
(C) Fan-Out Limitations **(D)** Both **(B)** & **(C)**

b. The poly silicon layer consists of

(A) Heavily Doped Silicon **(B)** Heavily Doped Poly Silicon
(C) Both **(A)** & **(B)** **(D)** None of these

c. The gate/channel capacitance is

(A) C_0WL **(B)** C_0/WL
(C) WL **(D)** C_gC_0

d. Figure of merit ω_0 is directly proportional to

(A) Width of channel **(B)** Length of channel
(C) Mobility of electron/hole **(D)** Electron Transit term

e. An inverter driven directly from the output of another should have a Zp.u/Zp.d ratio of

(A) $\geq 4/1$ **(B)** $\leq 8/1$
(C) $\leq 4/1$ **(D)** $\geq 8/1$

f. In Lambda based rules, λ is related to

(A) Interconnect Length **(B)** Oxide Layer
(C) Poly Layer **(D)** Resolution of the process

g. Deposition of metal or metal/silicon alloy is done in

(A) Sputtering **(B)** Evaporation
(C) Co-sputtering & Co-evaporation **(D)** All of these

h. In order to achieve symmetrical operation using minimum channel length, we would need to make

(A) Wp = 2.5 Wn **(B)** Wp=Wn
(C) Both **(A)** & **(B)** **(D)** None of these

i. The gate area of the device is

(A) $A_g = C_{ox}$ L W **(B)** A_g = L W
(C) $A_g = LW/C_{ox}$ **(D)** $A_g = C_oL$

j. Optimization of Time can be achieved in _____ design style.

(A) Full custom **(B)** Semi custom
(C) ASIC **(D)** Gate array

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Write down the different levels of integration of IC industry. **(4)**

b. With neat sketch explain briefly PMOS & NMOS enhancement mode transistor. **(8)**

c. Enlist the masks sequence in CMOS p-well process. **(4)**

Q.3 a. Define Stick Diagram. Explain the NMOS encodings in it. **(8)**

b. Implement schematic, stick diagram and corresponding layout of nMOS depletion load inverter. **(8)**

Q.4 a. Draw and explain nMOS depletion mode transistor pull-up and transfer characteristics. **(8)**

b. Explain the functionality of BiCMOS Drivers. **(8)**

Q.5 a. Explain the procedure to calculate sheet resistance of MOS transistors. **(8)**

b. Define sheet resistance and standard unit of capacitance $\square C_g$. Find the static and dynamic resistance of a minimum sized CMOS inverter. **(8)**

Q.6 a. Explain the Limits of miniaturization and Limits of interconnect and contact resistance. **(8)**

b. Draw and explain typical VLSI design flow in three domains (Y –Chart). **(8)**

Q.7 a. Enlist the CMOS subsystem design process steps. **(8)**

b. Draw and explain 4-bit ALU functions implementation with an adder. **(8)**

Q.8 a. Write the circuit of CMOS pseudo static memory cell and explain briefly working of it. **(8)**

b. Explain the optimization of nMOS inverter. **(8)**

Q.9 a. Explain different aspects of CAD Design Tools. **(8)**

b. Explain the advantages & disadvantages of implementing BIST include. **(8)**