ROLL NO. _____

Code: AE54/AC54/AT54/AE104 **Subject: LINEAR ICs & DIGITAL ELECTRONICS**

AMIETE – ET/CS/IT (Current & New Scheme)

Time: 3 Hours **JUNE 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. If the base currents for the emitter coupled transistors of a differential amplifier are $18\mu A$ and $22\mu A$, then the input bias current is

(A) $11\mu A$ **(B)** $20\mu A$
(C) $11mA$ **(D)** $22mA$

b. An OPAMP with a slew rate of $0.5V/\mu s$ is used in an application. The minimum time required for the circuit to change the output by 7V is

(A) $14\mu s$ **(B)** $41\mu s$
(C) $14ms$ **(D)** $41ms$

c. The common mode input to a certain differential amplifier, having a differential gain of 125 is $4\sin 200\pi t$ volts. The common mode output if CMRR is 60dB

(A) $0.5\sin(200\pi t)$ **(B)** 0
(C) 1 **(D)** None of these

d. In the circuit shown, in Fig.1, which LED glows if V_i = 1V

(A) Red LED
(B) Green LED
(C) Both Red LED and Green LED
(D) Neither Red LED nor Green LED

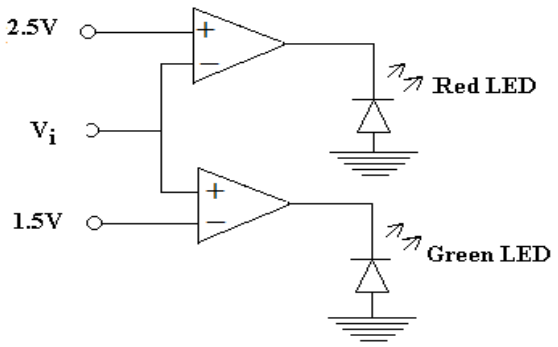

Fig.1

e. For a particular regulator, the output voltage on no load is observed as 10V while the full load output voltage is observed is 9.8 V. Then the load regulation is

(A) 2.04% **(B)** 1.02%
(C) 1% **(D)** 0

f. $(214)_{10} = (\ )_{16}$

(A) A6 **(B)** B6
(C) C6 **(D)** D6

g. Grady code of 15 is

(A) 1000 **(B)** 0001
(C) 1010 **(D)** 0101

h. The minimum expression for the Boolean function, $Y(A,B,C) = \sum m(0,2,4,6)$ is

(A) C **(B)** $\overline{C}$
(C) A **(D)** B

i. The output Q_n of a J-K flip-flop is 0. It changes to 1 when a clock pulse is applied. The inputs J_n and K_n are respectively

(A) 1 and X **(B)** 0 and X
(C) X and 0 **(D)** X and 1

j. The minimum number of NAND gates required to implement $A + A\overline{B} + A\overline{B}C$ is equal to

(A) 0 **(B)** 1
(C) 4 **(D)** 7

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

Q.2 a. Write a note IC's classification. **(4)**

b. Reason out why integrators are preferred over differentiators in analog computers. **(2)**

c. With the help of a functional block diagram, explain the working of an OPAMP. **(6)**

d. An amplifier has a differential gain of 400 and CMRR of 50 dB. If $V_{in1} = 50mV$, $V_{in2} = 60mV$ and $V_{noise} = 5mV$, determine the differential output and common mode output. **(4)**

Q.3 a. Realize a non-inverting summer using OPAMP. **(6)**

b. Discuss about frequency compensation of OPAMPs. **(6)**

c. What are the requirements of a good instrumentation amplifier? **(4)**

Q.4 a. With relevant equations show how OPAMP could be used as an integrator. **(5)**

b. Design an OPAMP Schmitt trigger for the following specifications. UTP = 2V, LTP = -4V and output voltage swings between $\pm 10V$. If the input is $V_i = 5 \sin \omega t$, plot the waveforms of the input and output. **(7)**

c. Differentiate between linear and non-linear operation of OPAMP. Give one example for each. **(4)**

Q.5 a. Suggest suitable values of resistors and reference voltage for a 4 - bit R - 2R ladder type DAC, if the resolution required is 0.5 **(4)**

b. With a neat sketch, explain the working of a successive approximation ADC. **(6)**

c. Discuss how OPAMP could be used as a free running oscillator. **(6)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 a. Discuss the advantages and limitations of digital techniques. **(8)**

b. Explain:
(i) BCD code (ii) Alphanumeric codes **(8)**

Q.7 a. Perform the following operations:
(i) $(5531)_8 - (3261)_8 + (100)_{10}$
(ii) Find 'x' in $(211)_x = (152)_8$ **(4)**

b. Minimize the following logic function using K-map and implement it using logic gates
$Y(A, B, C, D) = \sum m(0,1,2,3,4,7,8,9,10,11,12,14)$ **(6)**

c. Realize a full subtractor using two half subtractors. **(6)**

Q.8 a. Implement a half adder using multiplexers. **(6)**

b. Design an edge-triggered J-K flip-flop using NAND, OR gates. Explain its operation for positive edge triggering. **(10)**

Q.9 a. What is race around condition and how it is eliminated? **(4)**

b. Compare synchronous and asynchronous counters. Find the maximum frequency of a clock pulse at which the 4-bit ripple counter operates reliably. Assume delay of the flip-flops as 40 ns and the pulse width of strobe signal is 25 ns. **(6)**

c. Discuss how shift registers could be used for the following applications:
(i) SIPO (ii) Ring Counter
(iii) Sequence generator **(6)**