ROLL NO. _____

Code: AC58/AT58
AC106/AT106

Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT (Current & New Scheme)

Time: 3 Hours

JUNE 2015

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. A source program is usually in

(A) Assembly language **(B)** Machine level language
(C) High-level language **(D)** Natural language

b. The small extremely fast, RAM's are called as

(A) Cache **(B)** Heaps
(C) Accumulators **(D)** Stacks

c. _____ bus structure is usually used to connect I/O devices

(A) Single bus **(B)** Multiple bus
(C) Star bus **(D)** Rambus

d. The control unit controls other units by generating

(A) Control signals **(B)** Timing signals
(C) Transfer signals **(D)** Command Signals

e. Von Neumann architecture is

(A) SISD **(B)** SIMD
(C) MIMD **(D)** MISD

f. Virtual memory consists of

(A) Static RAM **(B)** Dynamic RAM
(C) Magnetic memory **(D)** Registers

g. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be

(A) 11 bits **(B)** 21 bits
(C) 16 bits **(D)** 20 bits

h. The interrupt-request line is a part of the

(A) Data line **(B)** Control line
(C) Address line **(D)** Information line

i. An n-bit microprocessor has

(A) n-bit program counter **(B)** n-bit address register
(C) n-bit ALU **(D)** n-bit instruction register

j. A three input NOR gate gives logic high output only when

(A) one input is high **(B)** one input is low
(C) two input are low **(D)** all input are high

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Discuss the bus structure of a computer system. **(4)**

b. How pipelining would improve the performance of CPU justify. **(4)**

c. Difference between control unit and main memory. **(4)**

d. Define Big-endian and Little-endian. **(4)**

Q.3 a. Register 'A' is having S-bit number 11011001. **(6)**

Determine the operand and logic micro-operation to be performed in order to change the value in 'A' to.
(i) 01101101
(ii) 11111101
(iii) Starting from an initial value R = 11011101, determine the sequence of binary values in R after a logical shift left, followed by circular shift right, followed by a logical shift right and a circular shift left.

b. Briefly explain instruction format. **(4)**

c. If a Computer has 128 operation codes and 512 k addresses, how many bits would be required for
(i) Single address instruction
(ii) Two address instruction **(6)**

Q.4 a. What do you mean by DMA channel? **(4)**

b. What is the sequence of steps that will take place when an interrupt occurs? **(6)**

c. When a DMA module takes control of bus and while it retain control of bus, what does the processor do? **(6)**

Q.5 a. Define interface circuit. Explain the function of an I/O interface. **(8)**

b. Describe Peripheral Component Interconnect (PCI) Bus Standards. **(8)**

Q.6 a. What do you mean by memory hierarchy? Explain cache memory. **(6)**

b. Differentiate between direct mapping and associate mapping. **(4)**

c. An 8-bit computer has a 16-bit address bus. The first 15 lines of address are used to select a bank of 32K bytes of memory. The higher order bit of address is used to select a register which receives the contents of the data bus? Explain how this configuration can be used to extend the memory capacity of system to eight banks of 32 K bytes each, for a total of 256 bytes of memory. **(6)**

Q.7 a. What are the advantages of virtual memory? **(4)**

b. Define the terms: Seek time, Rotational Delay, Access time. **(6)**

c. Design a half adder as a 2 level AND OR circuit. Implement full adder circuit using 2 half adder. **(6)**

Q.8 a. Explain the process of carry-save addition of summands. **(8)**

b. Explain restoring division and non-restoring division process. Also, give the algorithms for the two process. **(8)**

Q.9 a. What do you understand by Fetch cycle, instruction cycle, machine cycle? **(6)**

b. With suitable figure, discuss multiple-bus organization. **(6)**

c. Write the control sequence for execution of the instruction Add(R3), R1. **(4)**