ROLL NO. _____

Code: AC103/AT103 Subject: ANALOG AND DIGITAL ELECTRONICS

AMIETE – CS/IT (New Scheme)

Time: 3 Hours **JUNE 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions selecting at least two from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. With forward bias to a pn junction, the width of depletion layer _____

(A) decreases **(B)** increases
(C) remains the same **(D)** none of these

b. The _____ filter circuit results in the best voltage regulation.

(A) choke input **(B)** capacitor input
(C) resistance input **(D)** none of these

c. The emitter of a transistor is _____ doped.

(A) lightly **(B)** heavily
(C) moderately **(D)** none of these

d. In voltage divider bias, operating point is 3V, 2 mA. If V_{CC} = 9 V, R_C = 2.2kΩ, what is the value of R_E?

(A) 2000 Ω **(B)** 1400 Ω
(C) 800 Ω **(D)** 1600 Ω

e. Negative feedback is employed in _____

(A) oscillators **(B)** rectifiers
(C) amplifiers **(D)** none of these

f. The Gray code for decimal number 6 is equivalent to

(A) 1100 **(B)** 1001
(C) 0101 **(D)** 0110

g. What is the binary equivalent of the decimal number 368?

(A) 101110000 **(B)** 110110000
(C) 111010000 **(D)** 111100000

h. The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either

(A) a NAND or an EX-OR **(B)** an OR or an EX-NOR
(C) an AND or an EX-OR **(D)** a NOR or an EX-NOR

i. The 2's complement of the number 1101101 is

(A) 0101110 **(B)** 0111110
(C) 0110010 **(D)** 0010011

j. Data can be changed from special code to temporal code by using

(A) Shift registers **(B)** counters
(C) Combinational circuits **(D)** A/D converters

PART (A)
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Draw and explain the V-I characteristics (forward and reverse biasing) of a pn junction. **(8)**

b. Draw and explain the I-V characteristics of a Zener diode. What are the two breakdown mechanisms in a Zener diode? **(8)**

Q.3 a. A full-wave rectifier with a center-tapped transformer supplies a dc current of 100mA to a load resistance of R=20Ω. The secondary resistance of the transformer is 1Ω. Each diode has a forward resistance of 0.5Ω. Determine the following:
(i) RMS Value of the signal voltage across each half of the secondary.
(ii) DC power supplied to the load.
(iii) PIV rating for each diode.
(iv) AC power input to the rectifier.
(v) Conversion efficiency **(8)**

b. Draw the positive and negative voltage clipper circuits. Explain its working along with the waveforms. **(8)**

Q.4 a. Explain the operation of NPN transistor with neat diagrams. **(8)**

b. Fig.1 shows the voltage divider bias method. Draw the DC load line and determine the operating point. Assume transistor to be Silicon. **(8)**

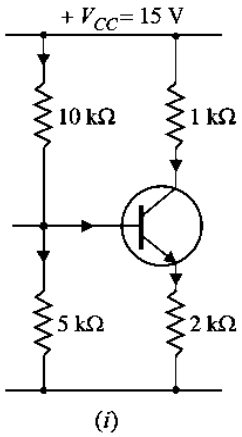

Fig. 1

Q.5 a. Draw the circuit of single stage CE amplifier and explain the function of bypass capacitor and coupling capacitors. **(8)**

b. Explain the working of Hartley oscillator with a neat circuit diagram. **(8)**

PART (B)

Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Explain the parallel and serial transmission of information in digital systems. **(8)**

b. What is the need for error detection and correction codes? Explain the parity method for error detection. **(8)**

Q.7 a. Prove the following identities using Boolean algebra: **(8)**

(i) $(A+B)(A+\overline{AB})C+\overline{A}(B+\overline{C})+\overline{A}B+ABC=C(A+B)+\overline{A}(B+\overline{C})$

(ii) $\overline{\overline{A(A\cdot B)}\cdot\overline{B(A\cdot B)}}=A\oplus B$

b. Reduce the following equation using k-map **(8)**

$$Y=\overline{A}\,\overline{B}\,\overline{C}+A\,\overline{C}\,\overline{D}+A\,\overline{B}+ABC\overline{D}+\overline{A}\,\overline{B}C$$

Q.8 a. Explain Full adder with an example. **(8)**

b. What is a decoder? Draw the logic circuit of a 3 line to 8 line decoder and explain its working. **(8)**

Q.9 a. With relevant diagram explain the working of master- slave JK Flip-Flop. **(8)**

b. Draw the diagram of a 4-bit synchronous up Counter and explain its working along with the waveforms. **(8)**