ROLL NO. _____

Code: AE74 **Subject: VLSI DESIGN**

AMIETE – ET

Time: 3 Hours **JUNE 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The speed power product of the basic logic gate circuit of NMOS technology is measured in

(A) picojoules **(B)** nanoseconds
(C) milli watts **(D)** mega Hertz

b. The value of electron surface mobility at room temperature is

(A) 240 cm^2/v sec **(B)** 650 cm^2/v sec
(C) 340 cm^2/v sec **(D)** 750 cm^2/v sec

c. The ratio of pull up to pull down registers for an NMOS inverter driven directly from output of another should have

(A) $\geq 8/1$ **(B)** $\geq 1/8$
(C) $\geq 4/1$ **(D)** $\geq 1/4$

d. The diffusion to diffusion separation in CMOS design process is

(A) 1λ **(B)** 2λ
(C) 3λ **(D)** 4λ

e. The overall propagation delay for n sections of a cascade pass transistor is

(A) $n^2rc\tau$ **(B)** nc□ c_g
(C) $rc\tau$ **(D)** $\alpha ne\tau$

f. The power dissipation per gate in MOS circuits is scaled by

(A) β/α^2 **(B)** $\frac{1}{\beta^2}$

(C) $\frac{\alpha^2}{\beta}$ **(D)** β^2

g. The regularity factor for a 4×4 bit shifter is

(A) 4 **(B)** 16
(C) 32 **(D)** 64

h. The dynamic power consumption in CMOS design is

(A) $\frac{C_L m.f}{V_{DD}^2}$ **(B)** $\frac{C_L m.f}{V_{DD}}$
(C) $mC_L V_{DD} f$ **(D)** $mC_L V_{DD}^2 f$

i. The delay associated with NMOS NAND is

(A) $n\ \tau_{inv}$ **(B)** $p\ \tau_{inv}$
(C) n/τ_{inv} **(D)** $\frac{p}{\tau_{inv}}$

j. The current in any bus branch along the length L of parent bus at a distance x from the source is

(A) $\frac{I_L}{L(1-x)}$ **(B)** $\frac{L}{I_L(1-x)}$
(C) $\frac{L(1-x)}{I_L}$ **(D)** $\frac{I_L(1-x)}{L}$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain basic n MOS transistors. **(8)**

b. Explain the thermal aspects of processing nMOS and CMOS devices. **(8)**

Q.3 a. Derive the relationship between transconductance and output conductance for MOS transistors. **(8)**

b. Explain CMOS inverter. **(4)**

c. Explain Bi CMOS Latch up susceptibility. **(4)**

Q.4 a. Explain contact cuts in NMOS circuits. **(8)**

b. Write down the double metal MOS process rules. **(4)**

c. Explain design rules for wires in 2 μm CMOS. **(4)**

Q.5 a. Calculate the rise time and fall time of a CMOS inverter. **(8)**

b. Explain the sources of capacitance which contribute to the overall wiring capacitance. **(8)**

Q.6 a. Derive an expression for depletion width. **(8)**

b. Explain the structured design of multiplexer. **(8)**

Q.7 a. Where the various approaches used at different stages of VLSI design process? Explain the basic architecture of 4 bit digital processor. **(8)**

b. Design a 4 bit adder. **(8)**

Q.8 a. What are the factors considered to make a comparative assessment of the dynamic shift registers? **(8)**

b. Explain floor plan layout of a 4- bit processor. **(8)**

Q.9 Write short note on: **(4×4)**

(i) Design Rule Checkers
(ii) CIF code
(iii) CAD Tools for design and simulation
(iv) Signature Analysis in BIST