ROLL NO. _____

Code: AE54/AC54/AT54 Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT

Time: 3 Hours **JUNE 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. CMRR of an Op-Amp should be _____

(A) zero **(B)** 1
(C) very low **(D)** very high

b. Slew rate of an Op-amp is expressed in _____

(A) V / Sec **(B)** V / μSec
(C) μV / Sec **(D)** μV / μSec

c. The instrumentation amplifier should have _____

(A) low input impedance **(B)** high output impedance
(C) high CMRR **(D)** all of these

d. In IC 555, pin No.7 is _____

(A) threshold **(B)** reset
(C) trigger **(D)** none of these

e. The fastest A to D converter is _____

(A) single slope type **(B)** flash type
(C) successive approximation type **(D)** dual slope type

f. $(1010110100111)_2 = (?)_{16}$

(A) AD38 **(B)** 15A7
(C) 16B7 **(D)** AD31

g. The number of rows in the truth table of 4 input AND gate will be _____

(A) 4 **(B)** 8
(C) 15 **(D)** 16

h. The number of bits needed to represent decimal values ranging from 0 to 500 are _____

(A) 8 **(B)** 9
(C) 10 **(D)** 11

i. Simplified expression of $y = (\overline{AB} + AB) \bullet (CD + \overline{CD})$ is _____

(A) 1 **(B)** 0
(C) A **(D)** $\overline{B}$

j. Simplified expression of $y = \overline{(ABCD) \bullet (\overline{ABCD})}$ is _____

(A) 1 **(B)** AB
(C) $A\overline{C} + \overline{B}D$ **(D)** 0

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

Q.2 a. Classify the integration technology as per the scale of integration. Explain in brief the various steps involved in fabrication of monolithic IC. **(10)**

b. Calculate (i) input bias current and (ii) input offset current for the circuit shown in Fig.1. Given that $\beta_1 = 100$ and $\beta_2 = 125$. **(6)**

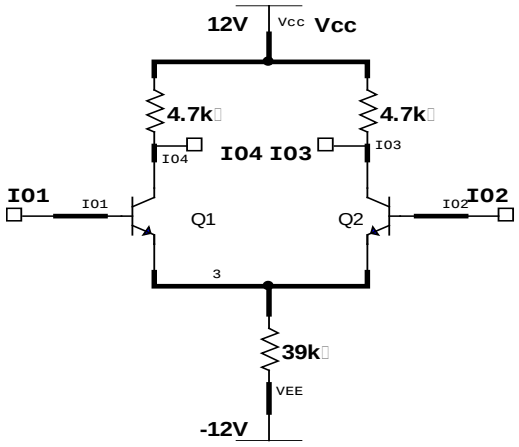

Fig.1

Q.3 a. What are the requirements of Instrumentation Amplifier? Draw 3-op-amp configuration of Instrumentation amplifier and derive the expression for its gain. **(9)**

b. The input V_i to an op-amp is 0.04 sin 1.13 x 10^5 t is to be amplified to the maximum extent. How much maximum gain required for an op-amp with a slew rate of 0.4 V/ μSec. **(7)**

Q.4 a. Draw and explain the ideal differentiator circuit. What are the problems associated with it and how are they eliminated in practical differentiator? **(8)**

b. Explain the operation of the circuit shown in Fig.2. Also draw the waveforms with suitable calculations by assuming $V_{sat} = 0.9V_{CC}$ **(8)**

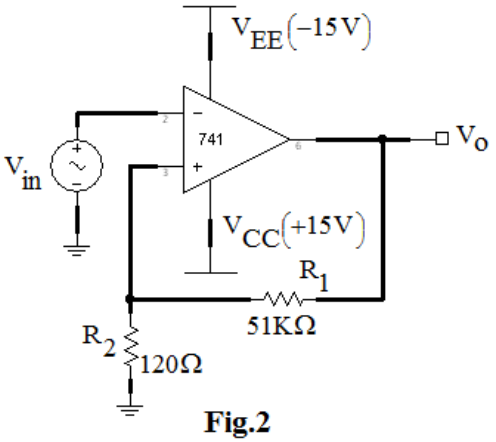

Fig.2

Q.5 a. State the disadvantages of Binary weighted resistor DAC and advantages of R-2R ladder network DAC. An 8 bit DAC has output voltage range from 0 to 5V, then find its resolution. **(8)**

b. Explain with suitable circuit diagram and waveforms Astable-multivibrator circuit operation using IC 555. **(8)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 a. Compare and contrast serial and parallel data transmission technique. **(6)**

b. A digital system consists of 1024 x 8 bit memory.
(i) How many address lines will it require?
(ii) Specify the range of address in Hex.
(iii) How many total number of bits can be stored in this memory? **(4)**

c. Make the following conversion (steps are necessary): **(6)**
(i) 100011101 to decimal
(ii) $(17735)_8$ to Hex
(iii) $(ABCD)_{16}$ to binary

Q.7 a. State and prove DeMorgan's Theorem. **(6)**

b. Implement the following expressions using NAND gates only. **(4)**
(i) Y = **A + B+ C.D**
(ii) Y = $\overline{A + B + C + D}$

c. Simplify the expression $Y = \Sigma m (0,1,2,3,7,8,9,10,11,12,13)$ using K-map and implement using basic gates. **(6)**

Q.8 a. Explain 1 digit BCD adder with suitable diagram. **(8)**

b. Explain the function of 8 : 1 multiplexer with the help of logic diagram and truth table. **(8)**

Q.9 a. Explain with waveforms, the implementation of 3 bit ripple counter using suitable flip-flops. **(8)**

b. Draw the diagram of four-bit bi-directional shift register using D flip-flops and explain its operation. **(8)**