ROLL NO. \_\_\_\_\_

Code: AE104

Subject: LINEAR ICs & DIGITAL ELECTRONICS

## AMIETE – ET {NEW SCHEME}

**Time: 3 Hours** 

# **JUNE 2014**

Max. Marks: 100

 $(2 \times 10)$ 

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions selecting at least TWO questions from each part, each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

#### Q.1 Choose the correct or the best alternative in the following:

a. The Slew Rate of an ideal Op-Amp is

(A) Zero	( <b>B</b> ) Infinity
(C) Low	(D) High

#### b. An instrumentation amplifier should have

<b>(A)</b>	High CMRR	( <b>B</b> ) Low CMRR
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- (C) High output impedance (D) High DC offset
- c. A Sample and Hold circuit is useful in

(A) Rectifier circuits	( <b>B</b> ) Digital interface circuits
(C) Amplifier circuits	( <b>D</b> ) Oscillator circuits

d. The 555 Timer is compatible with

(A) Only TTL circuits	( <b>B</b> ) Only CMOS circuits
(C) Both TTL & CMOS circuits	<b>(D)</b> Neither TTL nor CMOS circuits

e. The number of comparators required for a 4-bit parallel comparator type A to D converter is

( <b>A</b> ) 3	<b>(B)</b> 5
( <b>C</b> ) 7	( <b>D</b> ) 15

f.  $(423)_{10} = (\ )_{16}$ (A) 1A7 (C) 1BF (D) 1AE Subject: LINEAR ICs & DIGITAL ELECTRONICS

g.  $x + \bar{x}y =$ 

(A) $\bar{x}y$	$(\mathbf{B}) \mathbf{x} + \bar{\mathbf{y}}$
$(\mathbf{C}) \mathbf{x} + \mathbf{y}$	(D) $\overline{x} + y$

h. Which of the following provides a high output whenever the two inputs are at the same level?

(A) OR operation	( <b>B</b> ) XOR operation
(C) NOR operation	( <b>D</b> ) XNOR operation

i. The output frequency of decade counter that is clocked from 50 KHz signal is

(A) 25 KHz	( <b>B</b> ) 12.5 KHz
(C) 6.25 KHz	( <b>D</b> ) 5 KHz

j. The number of Flip-Flops required for constructing a Mod – 10 counter is

(A) 2	<b>(B)</b> 3
( <b>C</b> ) 4	<b>(D)</b> 5

## PART (A) Answer at least TWO Questions. Each question carries 16 marks.

- Q.2 a. Write about IC chip size and circuit complexity and explain power supply connections of an Op-Amp. (10)
  - b. Calculate  $i_1, v_0, i_L$  and total current is into the output pin of the circuit shown below in Fig.1 (6)



Q.3 a. Draw and explain the internal circuit of op-Amp. Explain the following terms:

- (i) Input Offset current(ii) Input Offset Voltage(iii) Slew rate(iv) Stability of Op-Amp
- b. Draw the circuit of instrumentation amplifier and derive the expression for its output.
  - (i) Using two Op-Amp (ii) Using three Op-Amp (8)

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- Q.4 a. Draw the circuit of Half-Wave rectifier using Op-Amp and explain. (8)
  - b. Explain the operation of practical differentiator circuit using Op-Amp. (8)
- Q.5 a. Explain the working of monostable multivibrator and derive the expression for the time period "T". (8)
  - b. Draw and explain the functional diagram of 555 Timer IC. Explain its application as pulse position modulator. (8)

## PART (B) Answer at least TWO Questions. Each question carries 16 marks.

Q.6	a.	Write the advantages of digital techniques and discuss serial and para transmission.	allel ( <b>8</b> )	
	b.	Explain the following codes:(i) BCD Code(ii) ASCII Code(iii) Gray Code(iv) Alphanumeric Code	(8)	
Q.7	a.	Construct a logic circuit for the following Boolean expression $Y = AC + B\overline{C} + \overline{ABC}$ using NAND gates only.	(6)	
	b.	b. Simplify the following logic expression using Karnaugh Map and explain		
		steps; $Y = \overline{C}(\overline{A}\overline{B}\overline{D} + D) + A\overline{B}C + \overline{D}$	(6)	
	c.	State De-Morgans Theorems. Obtain $\overline{A(BC + \overline{D}E + \overline{FG})}$	(4)	
Q.8	a.	Explain BCD adder with a neat diagram.	(4)	
	b.	Implement full adder using $3 \times 8$ decoder.	(6)	
	c.	Obtain 16:1 MUX using 2:1 multiplexers only.	(6)	
Q.9	a.	Design a synchronous counter using JK Flip-Flop that has the follow sequence: 000, 010, 101, 110 and repeat. The undesired states 001, 011, and 111 must always go to 000 on the next clock pulse.	ving 100 ( <b>8</b> )	
	b.	Explain, with a neat diagram and waveforms, the working of a Mod-6 John counter.	ison (8)	