ROLL NO. _____

Code: AC58/AT58 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT

Time: 3 Hours **JUNE 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. A _____ translates a high-level language program into sequence of machine instruction.

(A) Compiler **(B)** Machine translator
(C) Program translator **(D)** Interpreter

b. 1 M is equivalent to

(A) 2^{10} **(B)** 2^{20}
(C) 2^{15} **(D)** 2^{30}

c. In a vectored interrupt

(A) The branch address is assigned to a fixed location in memory.
(B) The interrupting source supplies the branch information to the processor through an interrupt vector.
(C) The branch address is obtained from a register in the processor
(D) None of these

d. When the I/O devices and the memory space share the same address space, the arrangement is called as _____.

(A) Memory-mapped I/O **(B)** Address controlled I/O
(C) Programmed memory I/O **(D)** Programmed I/O

e. Which is used to connect the processor to I/O devices that require transmission of data one bit at a time?

(A) Parallel port **(B)** Bridge
(C) Input-output interface **(D)** Serial port

f. A 16-bit computer that generates 16-bit addresses is capable of addressing upto _____ memory locations.

(A) 16K **(B)** 64K
(C) 1028K **(D)** 16M

g. Arithmetic shift left operation

(A) Produces the same result as obtained with logical shift left operation.
(B) Causes the sign bit to remain always unchanged.
(C) Needs additional hardware to preserve the sign bit.
(D) Is not applicable for signed 2's complement representation.

h. The method for updating the main memory as soon as a word is removed from the cache is called as

(A) Write-through
(B) Write-back
(C) Protected write
(D) Cache-write

i. Zero address instruction format is used for

(A) RISC architecture
(B) CISC architecture
(C) Von-Neumann architecture
(D) Stack-organized architecture

j. The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 1011101. What is the content of the register after each shift?

(A) 1110, 0111 **(B)** 0001, 1000
(C) 1101, 1011 **(D)** 1001, 1001

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Describe the characteristics of various generations of computer? **(6)**

b. What are the commonly flags used by the processor to keep track the information about the results of various operations? **(5)**

c. Consider the following instruction:
$C \leftarrow [A] + [B]$
Explain the two-phase execution procedure of the statement? **(5)**

Q.3 a. Explain the following addressing modes with examples:

(i) Immediate mode
(ii) Relative mode
(iii) Auto increment **(3×3)**

b. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of the seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and number of bits in each field if the instruction is in one word memory. **(7)**

Q.4 a. What is the disadvantage of transferring data through strobe control method? How handshaking overcomes this disadvantage? Explain. **(8)**

b. Define exception? Explain the different kinds of exceptions. **(8)**

Q.5 a. Describe the main phases involved in the operation of the SCSI bus. **(8)**

b. Draw and explain USB packet formats and frames. **(8)**

Q.6 a. Consider a memory consisting of 64K words of 8 bits each. Give the organization to implement this memory using 16K X 1 static memory chips.**(8)**

b. Explain the need of memory hierarchy with the help of a block diagram? What is the reason for not having one large memory unit for storing all information at one place? **(8)**

Q.7 a. Define and draw the logic diagram of n-bit ripple-carry adder. **(6)**

b. Why page-table is required in a virtual memory system. Explain different ways of organizing a page table. **(6)**

c. Write short notes on DVD Technology? **(4)**

Q.8 a. Multiply the following pairs of signed 2's-complement numbers using:
(i) Booth algorithm
(ii) Bit-pairing of the multiplier

A = 010111 and B = 110110
Assume A is the multiplicand and B is the multiplier. **(5+5)**

b. Discuss any two IEEE standard floating point formats. Explain Add/Subtract and multiply rules on floating point numbers. **(6)**

Q.9 a. Consider the statement ADD (R2), R1.
(i) Write the steps required for execution of above instruction?
(ii) Write the sequence of control steps required to perform the execution of above instruction for single bus architecture? **(6)**

b. With the help of block diagram, describe the complete processor? **(6)**

c. Compare and contrast between horizontal and vertical approach of microinstruction? **(4)**