ROLL NO. _____

Code: DE67 / DC67 **Subject: EMBEDDED SYSTEMS**

DipIETE – ET/CS (NEW SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. A Design metric of an embedded system is a

(A) Measure of performance **(B)** Measure of Response Time
(C) Measure of cost and size **(D)** All the above

b. In an digital camera, CCD is a

(A) Coupling Capture Device **(B)** Co-processor Capture Device
(C) Charge Coupled Device **(D)** Both **(A)** and **(B)**

c. A single chip with multiple processors is often referred to as a

(A) ASIC **(B)** ADSP
(C) SOC **(D)** Both **(A)** and **(B)**

d. The CACHE is usually designed using SRAM rather than DRAM because

(A) Cost
(B) Performance
(C) Appears on the same chip as a processor
(D) Both **(A)** and **(B)**

e. An 8 x 1 multiplexor has how many data inputs and select lines respectively

(A) 3 and 1 **(B)** 8 and 1
(C) 8 and 3 **(D)** None of the above

f. The Scheduling, Allocation and Binding are highly

(A) Interdependent **(B)** Independent
(C) Both **(A)** and **(B)** **(D)** None of the above

g. The Sensor networks are large-scale embedded systems that may contain

(A) Millions of nodes **(B)** Billions of nodes
(C) Thousands of nodes **(D)** Both **(A)** and **(C)**

h. In a fixed priority arbitration, each peripheral has a

(A) Unique Rank **(B)** Set of Ranks
(C) Low ranked **(D)** High ranked

i. The job of scheduler is

(A) shifting of tasks **(B)** keeping track of the tasks
(C) Both **(A)** and **(B)** **(D)** None of the above

j. Components that are commonly used in embedded software

(A) The State Machine **(B)** The Circular Buffer
(C) The Queue **(D)** All the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is a "market window" and why it is so important for products to reach the market early in this window. **(8)**

b. List and define the three main design technologies. **(8)**

Q.3 a. Design a combinational circuit for a problem "y is 1 if a is 1, or b and c are 1, z is 1 if b or c is 1, but not both". **(8)**

b. Define Optimization? Explain optimization opportunities in a single-purpose processor. **(8)**

Q.4 a. Explain Pipelining, Superscalar and VLIW Architecture. **(8)**

b. Draw and explain general software development design process. **(8)**

Q.5 a. Explain OTP ROM and EPROM with their suitable diagrams. **(10)**

b. What are the methods used by a microprocessor to determine the address of ISR? **(6)**

Q.6 a. Define arbitration method and explain any one. **(6)**

b. Draw a block diagram of a processor, memory, peripheral, and DMA controller connected with a system bus. Explain DMA write and read cycles. **(10)**

Q.7 a. Explain the example of ATM timeout using a watchdog timer. **(6)**

b. Explain the concept of PWM using suitable examples. **(10)**

Q.8 a. Explain the Process and Task concepts in RTOS. **(8)**

b. Draw the State transition graph for an I^2C bus master and explain it. **(8)**

Q.9 a. List the specifications in brief for an automatic chocolate vending machine (AVCM). **(8)**

b. Draw and explain hardware architecture of an AVCM. **(8)**