ROLL NO. _____

Code: DE60/DC68 Subject: MICROPROCESSORS & MICROCONTROLLERS

DipIETE – ET/CS (NEW SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. In Intel's 8085 microprocessor, the range of operating frequency is _____.

(A) 500 Hz to 3 MHz **(B)** 500 KHz to 3 MHz
(C) 50 KHz to 3 MHz **(D)** 5 KHz to 3 MHz

b. Intel's 8085 microprocessor has_____ address lines and can address a maximum of _____ memory.

(A) 8, 64 KBytes **(B)** 16,8 KBytes
(C) 32, 64 KBytes **(D)** 16, 64 KBytes

c. Intel's 8085 microprocessor has instruction size ranging from _____to _____.

(A) 0 to 4 bytes **(B)** 0 to 3 bytes
(C) 1 to 3 bytes **(D)** 1 to 6 bytes

d. In Intel's 8255, the specialty of Port-C is _____.

(A) BSR mode and two 4-bit ports **(B)** BSR mode and two 8-bit ports
(C) BSR mode and Bidirectional I/O **(D)** None of the above

e. In Intel's 8253, the following statement isFALSE.

(A) Operating frequency ranges from 0 Hz to 2 MHz
(B) The three timers T1, T2 and T3 are independently controlled
(C) 6 modes of operation including Mono-shot and square wave generation
(D) None of the above

f. In Intel's 8259, the INT signal is generated based on the inputs available from ____.

(A) ISR, IMR, IRR and Priority resolver
(B) IMR and, IRR only
(C) Priority resolver alone
(D) ISR, IMR and Priority resolver, but not IRR

g. Intel's 8051 MC can be interfaced with a maximum _____ data memory and _____ code memory.

(A) 64 Kbytes, 64 Kbytes **(B)** 16 Kbytes, 64 Kbytes
(C) 64 Kbytes**,** 32 Kbytes **(D)** 8Kbytes, 64 Kbytes

h. In Intel's 8051 MC status register, 'F0' bit is_____ and 'Ov' bit is_____.

(A) not used, over flow flag
(B) over flow flag, not used
(C) general purpose flag, over flow flag
(D) general purpose flag, not used

i. In Intel's 8051 MC, size of SP register is _____ and PC register is _____.

(A) 16 bits, 16 bits **(B)** 16 bits, 8bits
(C) 8bits, 16 bits **(D)** 8bits, 8bits

j. In Intel's 8051 MC, the following statement is TRUE regarding the two Timers.

(A) T1 is an up-counter and T2 is a down-counter
(B) Both T1 and T2 have4 modes of operation
(C) T1 is a down-counter and T2 is an up-counter
(D) T1 has 4 modes of operation and T2 has 3 modes of operation

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Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What are the salient features of the INTEL's-8085 microprocessor? Explain with a neat block diagram. **(10)**

b. What are the functions of the following pins of INTEL's-8085? **(6)**
(i) READY
(ii) SID and SOD
(iii) HOLD and HLDA

Q.3 a. What are the addressing modes available in INTEL's-8085? Explain with an example for each. **(8)**

b. What are the different instructions types available in INTEL's-8085? Explain with an example for each. **(8)**

Q.4 a. Correct the following instructions if necessary and indicate its addressing mode. **(8)**
(i) MOV B, B
(ii) OUT 1234h
(iii) LDAX, 1234h
(iv) PUSH A

b. Using 8085 instructions, write an assembly language program to interchange the contents of two arrays of bytes starting from locations "x" and "y". Write necessary comments. **(8)**

Q.5 a. When interrupted by an external interrupt what happens to the program execution in INTEL's-8085? Explain. **(8)**

b. What are the interrupt related instructions available in INTEL's-8085? Explain **(8)**

Q.6 a. What are the modes of operation for INTEL's-8255? Explain. **(8)**

b. Interface a logic controller to MP-8085 and write an assembly language program to realize a full adder. Write necessary comments. **(8)**

Q.7 a. Using a neat block diagram explain the internal architecture of INTEL's-8259. **(8)**

b. What is a DMA? Explain Burst mode and cycle stealing methods briefly. **(8)**

Q.8 a. Using a neat block diagram explain the internal architecture of INTEL's-8253. **(10)**

b. What are the features of INTEL's – 8251 USART? **(6)**

Q.9 a. What are the salient features of 8051 micro-controller? Explain with a neat block diagram. **(8)**

b. Write an assembly language program to interchange two blocks of data bytes using 8051 instructions. Write necessary comments for the same. **(8)**