ROLL NO. _____

Code: AE54/AC54/AT54 Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT (NEW SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The hexadecimal equivalent of binary number 1 1 1 0 1 1 0 1 1 1 1 0 1 0

(A) EDEB **(B)** 35572
(C) FB72 **(D)** 3B7A

b. An operational amplifier is acting as inverting amplifier has $R_1 = 10\,k\Omega$ $R_f = 100\,k\Omega$, the gain for the amplifier is

(A) –5 **(B)** 5
(C) 10 **(D)** –10

c. Common Mode Rejection ratio (CMRR) is

(A) $\left|\frac{A_{CM}}{A_{DM}}\right|$ **(B)** $\left|\frac{1}{A_{CM}}\right|$

(C) $\left|\frac{1}{A_{DM}}\right|$ **(D)** $\left|\frac{A_{DM}}{A_{CM}}\right|$

d. The output expression for the given circuit (Fig.1)

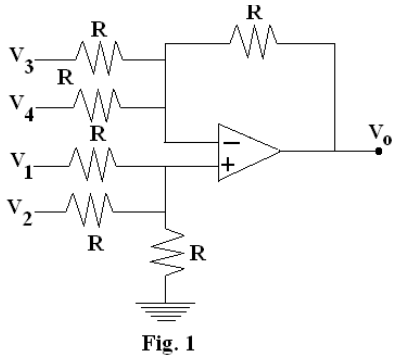


Fig. 1

(A) $V_0 = (V_3 + V_4) - (V_1 + V_2)$ **(B)** $V_0 = (V_1 + V_2) - (V_3 + V_4)$
(C) $V_0 = (V_3 + V_1) - (V_4 + V_2)$ **(D)** $V_0 = (V_4 + V_1) - (V_3 + V_2)$

e. The circuit (Fig. 2) given is

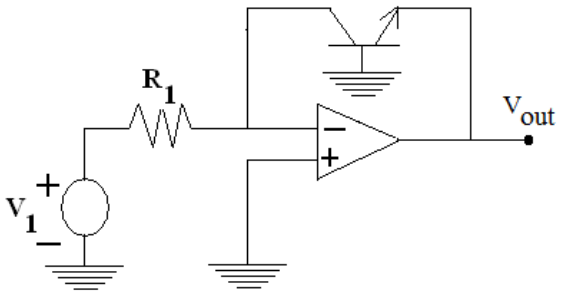


Fig. 2

(A) Antilog amplifier circuit **(B)** Peak clipper circuit
(C) Peak clamper circuit **(D)** Log amplifier

f. The maximum +ve and –ve numbers which can be represented by using 2's complement form using n bits is

(A) $+(2^n-1)$, $-(2^{n-1}-1)$ **(B)** $+2^{n-1}, -(2^{n-1}-1)$
(C) $+2^{n-1}, -2^{n-1},$ **(D)** $+(2^{n-1}-1), -2^{n-1}$

g. The parity of binary number is 1 1 0 0 1 1 0 is

(A) Even **(B)** Odd
(C) Same as the number of bits **(D)** Same as the number of zeros

h. The output frequency of an astable multivibrator (555) is

(A) $f = \frac{1}{T} = (R_A + 2R_B)C$ **(B)** $\frac{1}{(R_A + 2R_B)C}$
(C) $\frac{1.45}{(R_A + 2R_B)C}$ **(D)** $\frac{1}{C}$

i. The number of 2 to 4 decoders required to make 4 to 16 decoders are

(A) 3 **(B)** 2
(C) 4 **(D)** 5

j. The ring counter consisting of 5 FFs will have

(A) 10 states **(B)** 5 states
(C) 2^5 states **(D)** 7 states

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

Q.2 a. List out any 8 important characteristics of an ideal operational amplifier. **(8)**

b. Classify the ICs on the basis of application device used and chip complexity. **(4)**

c. In Fig. 3, given R_1 = 10 kΩ, R_f =100 kΩ, V_i = 1 V, a load of 25 kΩ is connected to the output terminal. Calculate (i) I_1 (ii) V_o (iii) I_L and total current I_o into the output pin (Fig. 3). **(4)**

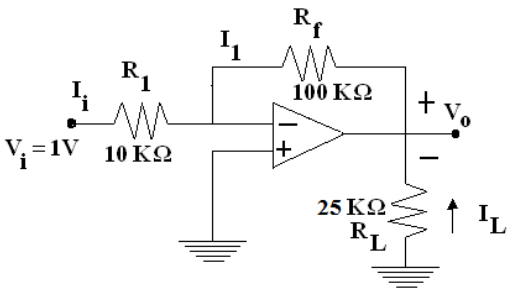
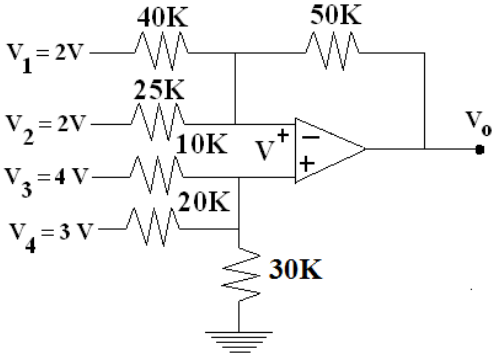


Fig. 3

Q.3 a. Define the terms (i) Input bias current (ii) Input offset current (iii) Input offset voltage (iv) Thermal drift. **(8)**

b. (i) Define slew rate of an opamp (ii) A square wave of peak to peak amplitude 800 mV has to be amplified to a peak to peak amplitude of 8 volts, with a rise time of 5 μs or less. Can 741 be used? Explain. **(8)**

Q.4 a. Find V_o for the adder-subtractor circuit given in Fig. 4. Draw the equivalent circuit for the steps.

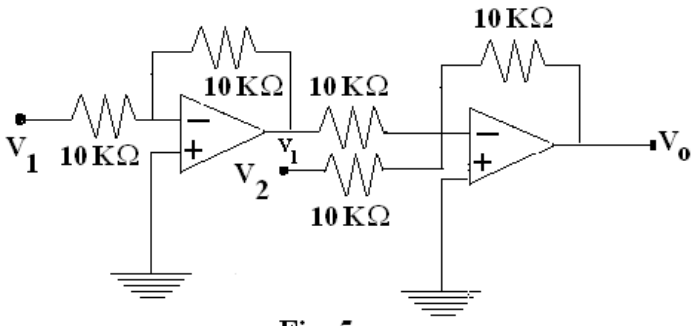


(6)

Fig. 4

b. Explain the operation of a practical integrator and draw the frequency response of a basic integrator showing the 0 dB gain cross over frequency. **(6)**

c. Calculate V_o for the circuit, given V_1=5 V, V_2 =2 V (Fig. 5).



(4)

Fig. 5

Q.5 a. Describe the operation of op-amp to generate an asymmetric square wave. **(6)**

b. The basic step of a 9 bit DAC is 10.4 mV (i) If 0 0 0 0 0 0 0 0 0 represents 0 V, what is the output produced if the input is $(1\ 1\ 1\ 1\ 0\ 1\ 1\ 1\ 1)_2$? (ii) What O/P voltage would be produced by a DAC, whose output range is 0 to 10 V, whose binary input number is (a) $(1\ 0\ 0\ 1\ 1\ 1\ 1\ 0)_2$ 8 bit DAC (b) $(1\ 0\ 1\ 1\ 0)_2$ 5 bit DAC **(2+4)**

c. Draw the internal functional diagram of 555 timer. **(4)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 a. Convert the following 8421 BCD numbers to their Excess-3 code equivalent.
(i) 0 1 1 0 0 0 0 0 (ii) 1 0 0 0 0 1 0 0 (iii) 1 0 0 1 0 0 1 1.
(iv) 0 1 0 1 1 1 0 0 **(4)**

b. Perform the following conversations: **(any 6)**
(i) $(1\ 1\ 0\ 1\ 0\ 1\ 1\ 0)_2$ =(____)$_8$ (ii) 472_8 =(____)$_2$
(iii) 0.325_8 =(____)$_{10}$ (iv) $(0\ 1\ 1\ 0\ 1\ 1\ 0\ 1)_2$ = (____)$_{16}$
(v) $(2040.125)_{10}$ =(____)$_{16}$ (vi) $(1\ 1\ 1\ 0\ 1.1\ 1\ 0\ 0\ 1)_2$ =(____)$_{10}$
(vii) B3F8.1=(____)$_{10}$ (viii) $(325.172)_{10}$=(____)$_8$ **(2×6)**

Q.7 a. Prove (A+BC)=(A+B)(A+C). **(2)**

b. Prove the following identity using De Morgan's theorem:
$\bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}xy\bar{z} + wy\bar{z} = \bar{z}(w + \bar{x} + \bar{y})$ **(4)**

c. Draw the logic circuit for the given identity: (i) $X = \overline{AB + C} + \overline{BC}$
(ii) $Y = \overline{AB + C} + B\bar{C}$ **(4)**

d. Implement the minimized boolean expression for the function:
(i) $f = b\bar{c}\bar{d} + \bar{a}bd + abd + bc\bar{d} + \bar{b}cd + \bar{a}\bar{b}\bar{c}d + a\bar{b}\bar{c}d$

(ii) $f = \bar{A}\bar{B}C + B\bar{C} + \bar{A}BC + ABC$ **(2×3)**

Q.8 a. Simplify the functions using K map (i) $X = \bar{A}\bar{D} + A\bar{B}\bar{D} + \bar{A}\bar{C}D + \bar{A}CD$
(ii) f(W,X,Y,Z)= $\sum(0,1,2,3,4,7,8,11,12,14,15)$ **(8)**

b. (i) Explain the operation of a BCD adder (ii) Subtract $(1\ 1\ 1\ 0\ 0)_2$ from $(1\ 0\ 0\ 1\ 1)_2$ using 2's complement subtraction. Also show direct subtraction for comparison. **(2×4)**

Q.9 a. Write short notes on:-
(i) Multiplexer (ii) Clocked JK FF **(2×4)**

b. Explain the operation of shift register counters. Aid your answer with suitable diagram. **(8)**