ROLL NO. _____

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. A combinational circuit with many inputs and outputs has many different paths, propagation delay of each path is

(A) Same **(B)** Different
(C) Same only for critical paths **(D)** Different only for critical paths

b. To make " Two ANDs and one OR " how many NANDs are required

(A) 4 **(B)** 3
(C) 2 **(D)** Not possible

c. Two's complement of a two's complement will return

(A) 0 **(B)** Same number
(C) Original number **(D)** none

d. Calculate the delay at an i-th stage in finding CY_i assuming that each stage of FA takes propagation time t_s.

(A) $2 . t_s$ **(B)** $2 .i . t_s$
(C) $2 / t_s$ **(D)** $i. t_s$

e. How many select lines will a 32:1 multiplexer will have

(A) 5 **(B)** 8
(C) 9 **(D)** 11

f. In an 1k x 8 ROM, number of address lines and data lines required are

(A) 8 and 8 **(B)** 12 and 8
(C) 10 and 8 **(D)** None

g. In VHDL, Configuration statement is used to

(A) Bind a entity and architecture
(B) Bind a components and functions
(C) Bind a packages and libraries
(D) Bind a component instance to an entity-architecture pair

h. The entity specifies

(A) The number of ports **(B)** The direction of ports
(C) The type of ports **(D)** All the above

i. The mechanism for delaying the new value is called

(A) Statement concurrency **(B)** Event scheduling
(C) Both **(A)** and **(B)** **(D)** None of the above

j. All the statements enclosed by the PROCESS are

(A) Concurrent statements **(B)** Sequential statements
(C) Configuration statements **(D)** None of the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain top-down and bottom-up approaches in digital systems hierarchical implementation. **(6)**

b. Use the tabulation method to generate the set of prime implicants for the following function
$f(x_1, x_2, x_3, x_4) = \Sigma(0,1,2,5,6,7,8,9,10,13,15)$ **(10)**

Q.3 a. Find a decomposition of
$f(x_1, x_2, x_3, x_4, x_5) = \Sigma(2,3,4,5,6,7,8,9,16,17,18,19,22,23,28,29)$ into
$F(G_1(x_1, x_3), G_2(x_2, x_5), x_4)$. **(10)**

b. Explain the properties of the symmetric function. **(6)**

Q.4 a. Explain all the design constructs of VHDL to describe logic. **(6)**

b. Write a VHDL code for describing function f = ab + cd using behavioral model. **(5)**

c. Write a VHDL code for describing full-adder using data-flow model. **(5)**

Q.5 a. Design 1-line-to-8-line Demultiplexer using basic logic gates. **(6)**

b. Design BCD synchronous counter using T- flip flop. **(6)**

c. Draw SR-Latch circuit using NOR gate and mention it's truth table. **(4)**

Q.6 a. Define FSM? Explain Mealy and Moore FSM. **(8)**

b. Explain state equivalence and machine minimization in sequential machines. **(8)**

Q.7 a. Using PLA implement Full –Adder functionality. **(6)**

b. Explain how PAL can be used in digital system design. **(6)**

c. (i) A given memory chip has 12 address pins and 4 data pins. Find the organization and Capacity.
(ii) Example 2: A 512K-memory chip has 8 pins for data. Find the organization and number of address pins for this memory chip. **(4)**

Q.8 a. What are the attributes in VHDL? List all types of attributes available in VHDL. **(8)**

b. Realize 13 variable symmetric function using 10 full adders and 1 decoder. **(8)**

Q.9 a. Define data subsystem. Explain all the important modules required to implement data subsystem. **(8)**

b. Draw the block diagram of micro-programmed controller and explain the importance of each unit in that. **(8)**