ROLL NO. _____

Code: AE13 **Subject: COMPUTER ENGINEERING**

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: **(2×10)**

a. CISC is characterized by

(A) Fixed length instructions **(B)** Variable length instructions
(C) No instructions **(D)** None of above

b. _____ code provides a way for decimal numbers to be encoded in a binary form that is easily converted back to decimal

(A) Gray **(B)** ASCII
(C) Parity codes **(D)** BCD

c. Which of the following is true?

(A) 8086 do not support segmented memory
(B) Segmentation needs extra hardware and software
(C) Data and extra segments belong to 8085
(D) Instruction queue degrades the performance of 8086

d. The storage cell of DRAM is actually a

(A) Battery **(B)** Resistor
(C) Capacitor **(D)** Inductor

e. An interrupt caused by an external signal applied to an interrupt input line of CPU is known as

(A) Firmware interrupt **(B)** Event interrupt
(C) Hardware interrupt **(D)** Software interrupt

f. Printers has an internal _____ and _____ is used to write bytes to this _____until BUSY flag is set.

(A) Schedule, lock, release **(B)** Sync, spool, buffer
(C) Spool, buffer, buffer **(D)** Buffer, polling, buffer

g. _____ memory is typically built using fast-responding static RAM located between the processor and main memory.

(A) Virtual **(B)** Protected
(C) Cache **(D)** RAID

h. The two's compliment of binary number is 1011 the original number is

(A) 1001 **(B)** 0100
(C) 0101 **(D)** 1010

i AT architecture is based on _____

(A) 8086 **(B)** 80386
(C) 80186 **(D)** 80286

j. The following is a valid feature of EISA architecture

(A) Supports multiple processors via bus arbitration
(B) Supports non-shareable interrupts
(C) 16-bit address and data bus widths
(D) Both **(A)** and **(B)**

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a Compare the features of hardware, software and firmware. **(6)**

b. Give Flynn's classification of computers. **(4)**

c. Explain the following and give their features:
i. Processor performance
ii. RISC
iii. Control and data flow computers **(6)**

Q.3 a. Give any three commands of both DOS and UNIX systems. **(6)**

b. Give the decimal format for each of the following numbers:
i. Hex FC3A
ii. Octal 7633
iii. Binary 10101011 **(3)**

c. Explain 8085 vectored interrupts. Write a program to enable RST 7.5 and 5.5. **(7)**

Q.4 a. Explain with a block diagram the working of 8085 processor. **(6)**

b. Draw the timing diagram of the following:
i. Fetch cycle
ii. Read cycle
iii. Write cycle **(6)**

c. Compare minimum mode and maximum mode of 8086. **(4)**

Q.5 a. Explain the characteristic features of the following processors:
i. Power PC
ii. SUN's Ultra SPARC
iii. AMD **(6)**

b. Draw the block diagram of P6 processor. Compare its performance with Pentium processor. **(6)**

c. Explain real, virtual and protected modes of 8086 processor. **(4)**

Q.6 a. Explain various memory technologies and their storage features. **(4)**

b. Give advantages and disadvantages of cache memory, associative memory and virtual memory. **(6)**

c. Explain features of raster, vector and bit mapped scan. **(6)**

Q.7 a. Draw the block diagram of programmable interrupt controller 8259. **(6)**

b. Explain six modes of 8254 programmable interval timer. **(6)**

c. Explain any two input devices with their working mechanism. **(4)**

Q.8 a. Compare and contrast the following bus structures:

i. ISA
ii. EISA
iii. PCI **(9)**

b. Calculate the time for one PC bus cycle, assuming a 6.78 MHz clock frequency. Calculate the data transfer rate of this bus? Assume I/O buscycle and 5 T states. **(3)**

c. Explain IRQ, DMA channels and I/O address in PC/XT and AT architectures. **(4)**

Q.9 a. Give the features of the following programmable peripheral interface:

i. *Detect* key stroke in key matrix
ii. *Debounce* the switch closure and release
iii. *Encode* key with a value **(6)**

b. Compare the features of various high level and low level programming languages. **(3)**

c. Write an assembly language program to find the maximum of two numbers. **(3)**

d. Mention any two data and control signals used in EISA bus. **(4)**