ROLL NO. _____

Code: AE09 **Subject: ANALOG & DIGITAL ELECTRONICS**

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The main advantage of using a three op-amp instrumentation amplifier over a single op-amp differential amplifier lies in

(A) higher value of CMRR
(B) lower noise figure
(C) Elimination of the need for accurate matching of resistors
(D) Simplicity of gain adjustment

b. A major advantage of active filters is that they can be realized without using

(A) op-amps **(B)** inductors
(C) resistors **(D)** capacitor

c. The number of comparisons carried out in a four bit flash type A/D converter is

(A) 16 **(B)** 15
(C) 4 **(D)** 3

d. Logarithmic amplifier are used in

(A) Adders **(B)** Dividers
(C) Multipliers **(D)** All of the above

e. A TTL circuit with totem pole output has

(A) Higher output impedance **(B)** Low output impedance
(C) Very high output impedance **(D)** Any of the above

f. Which of the following circuit can be used as parallel to series converter?

(A) Digital converter **(B)** Decoder
(C) De-multiplexer **(D)** Multiplexer

g. Which of the following flip-flop is used as latch?

(A) JKFF **(B)** DFF
(C) SRFF **(D)** TFF

h. If an NMOS acting as a switch in depletion mode then

(A) The device is cut-off for $V_{GS}=0$
(B) The device is cut-off for low V_{DS}
(C) The device is cut-off for large negative V_{GS}
(D) The device is in saturation high values of V_{DS}

i. The internal structure of PLA is similar to

(A) RAM **(B)** ROM
(C) Both ROM and RAM **(D)** Neither RAM nor ROM

j. RAM can be expanded to

(A) Increase word size **(B)** Increase word number
(C) Both **(A)** and **(B)** **(D)** None of the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw and explain the architecture of an NMOS op-amp. Give three reasons as why this architecture is employed. **(8)**

b. For the circuit shown in Fig. 1, find the differential voltage gain $A=Vo/(V_1-V_2)$. **(8)**

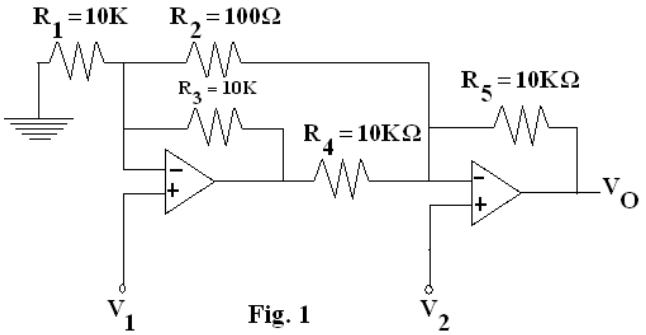

Fig. 1

Q.3 a. Find the Chebyshev transfer function for the low pass filter that meets the specification
f_P=10 kHz, A_{max}=1 dB, f_S=15 kHz, A_{min}=25 dB, dc gain=1 **(8)**

b. What are the advantages of switched capacitor filter? Draw the switched-capacitor form of an active BP filter. **(8)**

Q.4 a. Draw the block diagram of dual slope A/D converter and explain its operations. **(10)**

b. Find V_0/V_1 for the op-amp circuit if $n \neq 1$ in Fig. 2.

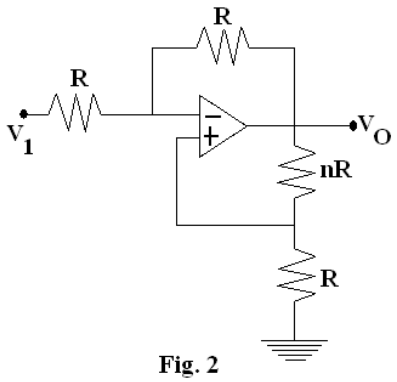

Fig. 2 **(6)**

Q.5 a. Explain how an FET can be used as a switch **(8)**

b. Explain the working of (i) CMOS NAND gate (ii) CMOS NOR gate. **(8)**

Q.6 a. Explain how a BJT act as an inverter. **(10)**

b. Explain the following:
(i) Bipolar logic family and unipolar logic family
(ii) Saturated and non saturated logic
(iii) Tristate logic **(2×3)**

Q.7 a. Simplify the following logic expression using Boolean Algebra:
(i) F=AB+A(B+C)+B(B+C)
(ii) $f = A\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,D + BC\overline{D} + \overline{A}B + B\overline{C}$ **(4×2)**

b. Design BCD to Gray code converter using 4:1 mux. **(8)**

Q.8 a. Design a synchronous mod-6 counter using JK flip-flop. **(10)**

b. What are the different forms of triggering in flip-flop? Explain each one with an example. **(6)**

Q.9 Write short note on any **TWO**:
(i) CCD
(ii) PLA
(iii) EPROMS **(8×2)**