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## AMIETE - CS/IT (NEW SCHEME)

Time: 3 Hours

## PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

## NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the $\mathbf{Q} .1$ will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.
Q. 1 Choose the correct or the best alternative in the following:
a. The two's complement of a binary number is 0011 . The decimal equivalent of the original number is
(A) 12
(B) 13
(C) 16
(D) 14
b. In 4 bit CLA addition process requires one
(A) 4 gate delay
(B) 3 gate delay
(C) 1 xor gate delay
(D) 2 gate delay
c. 5 data bytes are pushed in to a RAM stack beginning at address $(11 \mathrm{BF})_{\mathrm{H}}$. What is top of the stack address after the data are loaded?
(A) $(11 \mathrm{C} 0)_{\mathrm{H}}$
(B) $(11 \mathrm{BA})_{\mathrm{H}}$
(C) $(11 \mathrm{~B} 0)_{\mathrm{H}}$
(D) $(1101)_{\mathrm{H}}$
d. Set associative mapping is related to
(A) Cache mapping
(B) Virtual memory
(C) DRAM
(D) None of the above
e. In bit pair recoding of multiplication the summands for $n$ bit operands
(A) $n / 2$
(B) $n$
(C) $n^{2}$
(D) $n / 4$
f. In logical right shifting, the fill in bits are always
(A) 1
(B) 0
(C) MSB must be repeated
(D) Sign bit must be repeated
g. In Multiprocessor systems
(A) Memory is shared between all processors
(B) Multiple processors are used
(C) Multiple computers are used
(D) Both (A) \& (B)
h. SPEC rating $=$
(A) $\frac{\text { Running time on reference computer }}{\text { Running time on the computer under test }}$
(B) $\frac{\text { Running time on test computer }}{\text { Running time on reference computer }}$
(C) None of the above
(D) Both (A) \& (B)
i. In I/O mapped I/O
(A) Memory and I/O share the entire address range
(B) Separate address for memory and I/O
(C) None of the above
(D) Both (A) \& (B)
j. DDR RAM has bandwidth
(A) Double that of SDRAM
(B) Half that of SDRAM
(C) Same as SDRAM
(D) Quarter as that of SDRAM


# Answer any FIVE Questions out of EIGHT Questions. <br> Each question carries 16 marks. 

Q. 2 a. Explain the features of a CISC processor in detail.
b. Consider the memory system of a computer storing the following data:

| Address in Hex | Data stored (binary) |
| :--- | :--- |
| 2000 | 00111000 |
| 2001 | 00110100 |
| 2002 | 00110010 |
| 2003 | 00111001 |

Interpret the storage as numbers.
(i) Little Endian storage in ASCII of 4 digit BCD word.
(ii) Big Endian storage of 2 BCD words of 4 digits each.
(iii) Big Endian storage of 2 hex numbers of 4 digits each.
(iv) Little Endian storage in ASCII of 4 digit signed hex words.
Q. 3 a. Explain various addressing modes with example of each.
b. What is a queue? Explain the various operations on queue.
Q. 4 a. Explain the various methods of I/O interfacing techniques.
b. How do you handle multiple interrupts and also explain vector interrupts.
Q. 5 a. Elaborate the features of PCI Bus.
b. Draw and explain USB tree structure.
Q. 6 a. A computer has 16 MB main memory and 64 KB cache. The block size is 16 bytes.
(i) How many cache lines does the computer have?
(ii) How many blocks does the main memory have?
(iii) Give the starting address of memory blocks which are directly mapped to cache lines.
(iv) Explain how a given address is retrieved from the memory system.
b. Draw and explain the organisation of 4 MB semiconductor memory constructed using $256 \mathrm{~K} \times 1$ chips.
Q. 7 a. Explain the various DVD formats and their applications.
b. Draw and explain the hardware implementation of unsigned binary multiplication with example.
Q. 8 a. Perform the given multiplication using Booth's recoding algorithm.

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\begin{equation*}
01110 \times 11011 \tag{8}
\end{equation*}
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b. What are special values and exceptions in IEEE floating point number system?
Q. 9 a. Give the formats for micro instruction and explain the fields.
(8)
b. What techniques are used by the computer designer to generate the control signal? Explain in brief.

