ROLL NO. _____

Code: AC07 / AT07 Subject: COMPUTER ARCHITECTURE

AMIETE – CS/IT (OLD SCHEME)

Time: 3 Hours **JUNE 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2 ×10)**

a. In logical shift left of a binary number in 2's complement form generates overflow if

(A) $A_n . A_{n-1} = 0$ **(B)** $A_n \oplus A_{n-1} = 0$
(C) $A_n \oplus A_{n-1} = 1$ **(D)** $A_n + A_{n-1} = 1$

b. Which of the following circuits are combinational?
(i) Adder
(ii) Multiplexer
(iii) Counter

(A) (i) and (ii) **(B)** (ii) and (iii)
(C) (i) and (iii) **(D)** (i), (ii) and (iii)

c. When is BSA instruction used?

(A) unconditional jump
(B) conditional jump
(C) subroutine execution
(D) jump when accumulator has signed number

d. A digital computer has a common bus for 16 registers of 32 bits each. The bus is constructed with multiplexers. What size of multiplexers are needed and how many multiplexers are there in the bus?

(A) 4 × 2; 32 **(B)** 16 × 1 ; 32
(C) 16 × 1; 16 **(D)** 16 ×4 ; 32

e. Which of the following is wrong with respect to subroutines?

(A) The address is saved before executing a subroutine so that control can be transferred back to the main program after execution of subroutines.
(B) The use of subroutines improves readability of the program
(C) Execution of subroutine uses stack
(D) All of the above

f. What does a sequence of micro instructions refers to?

(A) micro operations **(B)** micro code
(C) micro program **(D)** both **(B)** or **(C)**

g. What is the result of the arithmetic operation (+52)+(–15) in binary using signed 2's complement representation?

(A) 100101 **(B)** 010100.
(C) 100100. **(D)** 101101.

h. Which of the following is wrong?

(A) During DMA transfer, CPU is busy executing an instruction.
(B) CPU delays its operation for one more memory cycle to allow DMA.
(C) DMA is used to increase I/O speed
(D) The bus request input is used by the DMA controller to request the CPU to relinquish control of the bus.

i. With which of the following is page replacement associated with?

(A) Cache memory **(B)** Secondary memory
(C) Virtual memory **(D)** Main memory

j. What is the decimal equivalent of 101110?

(A) 64 **(B)** 34
(C) 46 **(D)** 44

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Simplify the following Boolean function in sum-of-products form by means of a four-variable map. Draw the logic diagram with
(i) AND-OR-Inverter gates; (ii) NAND gates.
$F(A,B,C,D) = \sum m(0,2,8,9,10,11,14,15)+\sum d(6,7)$ **(8)**

b. What are the steps that are carried out to store a data in a memory location? Give the logic diagram to address a location in 4×16 memory array. **(6)**

c. Convert the hexadecimal number F3A7C2 to binary and octal. **(2)**

Q.3 a. The 8-bit registers AR, BR, CR and DR initially have the following values:
AR = 11110010
BR =11111111
CR = 10111001
DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

AR← AR +BR	Add BR to AR
CR← CR^ DR, BR←BR + 1	AND DR to CR, increment BR
AR ← AR – CR	Subtract CR from AR

(6)

b. An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 1011100, determine the register value after an arithmetic shift left, and state whether there is an overflow. **(4)**

c. With a diagram, explain how a BCD adder works. **(6)**

Q.4 a. With neat diagram of a common bus system, show how to execute the micro-operation AC ← AC+DR. **(6)**

b. A Stack is organized in such that SP always points at the next empty location on the stack. List the micro operations for the push and pop operations. Assume stack grows downwards. **(4)**

c. Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical result. (3+4)*[10*(2+6)+8]. **(2+4)**

Q.5 a. Explain how programmed I/O and interrupt initiated I/O operations are carried out. **(8)**

b. Describe in detail how data is transferred in using DMA. Draw necessary diagrams to support your explanation. **(8)**

Q.6 Explain the basic organization of micro programmed controller and its working. State its advantage over hardware control unit. **(16)**

Q.7 a. Explain Booth's algorithm with flow chart and show the data flow in each step for multiplying (–7)×(–5). **(10)**

b. Perform the subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend.
(i) 5250 -1321 (ii) 1753 - 8640 **(6)**

Q.8 a. What is the need for Virtual memory organization? Explain different mapping techniques used. **(10)**

b. Discuss page replacement policies. **(6)**

Q.9 a. Construct a 5-32 line decoder with four 3-to-8 decoder with enable and one 2-to-4 decoder. **(8)**

b. How many 128 × 8 memory chips are needed to provide a memory capacity of 4096 × 16? Give the circuit diagram of the memory using the memory chips. **(8)**