ROLL NO. _

Code: DE67/DC67/DE115/DC121

Subject: EMBEDDED SYSTEMS

DiplETE – ET/CS (Current & New Scheme)

Time: 3 Hours

June 2019

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1	Choose the correct or the best alternative in the following:		(10×2)	
	a. The time between the task's execution and the end is called as			
	(A) Throughput	(B) Latency		
	(C) Performance	(D) Concurrency		
	b. Multiplexer in Combinational components is also called as			
	(A) Register	(B) Selector		
	(C) Decoder	(D) Adder		
	c. Which of the following steps is not involved in execution of instruction			
	(A) Cache Hit	(B) Decoding		
	(C) Storing	(D) None of these		
	d. To achieve 75% duty cycle to run a DC motor at 6900 RPM we need to load into the cycle_high of PWM			
	(A) 7FH	(B) BFH		
	(C) CCH	(D) 89H		
	e. In EDO DRAM, EDO stands for			
	(A) Enhanced Data out	(B) Extra Data Out		
	(C) Extended Data out	(D) None of these		
	f. To obtain a duration of 3 microsecond from a clock cycle of 10 nano second, the number of clock cycles required are			
	(A) 333	(B) 303		
	(C) 300	(D) 330		
	g. Priority Arbiters typically uses which of the common scheme to determine priority among peripherals?			
	(A) Fixed priority	(B) Rotating priority		
	(C) Both (A) and (B)	(D) None of these		

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	h. IEEE 1394 has given the specification of	f following protocol			
	(A) Firewire (I) (C) IrDA (I)	B) FC D) Bluetooth			
	i Which of the following lover provides I	PC in Comoro system?			
	(A) Application (I	B) System			
	(C) Control (I	D) Base			
	j. Which of the following defines the set of	of instructions loaded into the memory?			
	(A) Process (I) (C) Thread	B) Task D) System hardware			
	Answer any FIVE Questions ou	it of EIGHT Questions.			
$\overline{02}$	Each question carries 16 marks.				
Q.2	a. State and explain common design men	an Embedded system.	(0)		
0.0	b. Explain the different characteristics of	an Embedded system.	(8)		
Q.3	a. Explain Scheduler with example.		(4)		
	b. Enlist and explain three methods of pro	otecting shared data w.r.t semaphore.	(4)		
	c. Exlplain RTOS semaphore.		(4)		
	d. Explain Semaphore as a signaling devi	ce.	(4)		
Q.4	a. Design a Combinational logic design for	or a half substarctor.	(8)		
	b. Distinguish between Sequential and combinational circuit. (4				
	c. Explain the purpose of datapath of cont	roller.	(4)		
Q.5	a. Explain the concept of pipelining. List	the factors of selecting a microprocessor.	(8)		
	b. Draw and explain architecture of a sim	ple microprocessor.	(8)		
Q.6	a. Explain ATM timeout using a watchdo	g timer.	(6)		
	b. Explain Controlling a DC motor using	PWM.	(6)		
	c. Explain Stepper motor controlling usin	g a driver.	(4)		
Q.7	a. State and explain different cache memo	ory mapping techniques.	(8)		
	b. Classify memory. Explain Flash memo	ry in detail.	(8)		
Q.8	a. Discuss memory mapped I/O method for	or communication.	(4)		
	b. Describe the following in detail.(i) IrDA (ii) PCI Bus (iii) I2C	(4	4X3)		
Q.9	a. Draw the software architecture of automatic chocolate vending machine (AVC				
	b. Explain different software layers in sof	tware architecture of a camera.	(8)		