**Subject: COMPUTER ORGANIZATION Code: DC57/DC107** 

### **DiplETE - CS (Current & New Scheme)**

**June 2019** Time: 3 Hours Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

**NOTE:** There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each

<b>Q.1</b>	Cł	hoose the correct or the best alternative in the following:		
	a.			
		(A) Accumulators	( <b>B</b> ) Registers	
		(C) Heap	(D) Stack	
	b.	A source program is usually in		
		(A) Assembly language	(B) Machine level language	
		(C) High level language	( <b>D</b> ) Natural language	
	c.	The format is usuall	y used to store data	
		(A) BCD	(B) Decimal	
		(C) Hexadecimal	( <b>D</b> ) Octal	
	d.	The time delay between two succ called	essive initiation of memory operation is	
		(A) Memory access time	<b>(B)</b> Memory search time	
		(C) Memory cycle time	( <b>D</b> ) Instruction delay	
	e.	Which register can interact with t	he secondary storage?	
		(A) MAR	<b>(B)</b> PC	
		(C) IR	$(\mathbf{D}) R_{o}$	
	f.	The register, ALU & the intercon as	nection between them are collectively called	
		(A) Process route	( <b>B</b> ) Information trail	
		(C) Information path	(D) Data path	
	g.	respectively. Suppose A can exec	clock frequencies of 700 MHz & 900 MHz ute an instruction with an average of 3 steps	
		& B can execute an instruction w	ith an average of 5 steps. For the execution	
		of the same instruction which pro	cessor is faster?	
		( <b>A</b> ) A	<b>(B)</b> B	
		(C) Both take the same time	( <b>D</b> ) Insufficient information	

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hbus structure is usually used to connect I/O devices					
(	(A) Single Bus	( <b>B</b> ) Multiple Bu	S		
(	(C) Star Bus	( <b>D</b> ) Ram Bus			
<ul> <li>i. The advantage of DMA is</li> <li>(A) Avoiding "busy waiting" by CPU</li> <li>(B) High- Speed data transfer between memory &amp; I/O</li> </ul>					
	· · ·				
•		fixed instruction size are the <b>(B)</b> RISC	e features of		
		_	stions.	_	
a. V	What are the functional ele	ements of a computer? Expla	in in detail.	(8)	
7	The instruction mix and th		_		
		Instruction%	СЫ		
	* ' *		2		
$\epsilon$	each:				
	-	by a new one that reduces	the total computation	l	
(ii)	The disc is replaced with	a solid state device that re-	duces the disk waiting	5	
p	erformance. The average f				
		best speed up?		(8)	
		ress instruction for the follow	wing expression:	(8)	
b. V	What is an instruction? Dis	scuss the instruction design s	et issues.	(8)	
	1	ure & an I/O interface for an	Input device using	(4+4)	
		What are its types. Explain us	sing suitable	(4+4)	
	i. 1. () () () () () () () () () () () () () (	<ul> <li>(A) Single Bus</li> <li>(C) Star Bus</li> <li>i. The advantage of DMA is</li> <li>(A) Avoiding "busy waiting (B) High- Speed data trans</li> <li>(C) Polling</li> <li>(D) None of these</li> <li>j. Few addressing modes and (A) CISC</li> <li>(C) RAID</li> <li>Answer any FIVE Quest Each quest</li> <li>a. What are the functional election of the instruction mix and the is:</li> <li>Type Int Floating Type Other</li> <li>Considering following 3 reach:</li> <li>(i) The processor is replaced time by 35%</li> <li>(ii) The disc is replaced with time by 85%</li> <li>(iii) The processor is replaced performance. The average of the are unchanged.</li> <li>Which modification gives the late which modification gives the late are unchanged.</li> <li>Which modification? Discussion of the late with the processor of the late of the late</li></ul>	i. The advantage of DMA is (A) Avoiding "busy waiting" by CPU (B) High- Speed data transfer between memory & I/O (C) Polling (D) None of these  j. Few addressing modes and fixed instruction size are the (A) CISC (C) RAID (D) None of the  Answer any FIVE Questions out of EIGHT Questach question carries 16 marks.  a. What are the functional elements of a computer? Expla  b. A computer spends 82% of its time in computing & 18 The instruction mix and the average cycle per instruction is:  Type Instruction% Int 40% Floating Type 30% Other 30% Considering following 3 modification to the system, each: (i) The processor is replaced by a new one that reduces time by 35% (ii) The disc is replaced with a solid state device that retime by 85% (iii) The processor is replaced with a new one that has in performance. The average floating point CPI is reduced are unchanged. Which modification gives the best speed up?  a. Write the zero and one address instruction for the follow X=A*(B-C)/(E+F-G)  b. What is an instruction? Discuss the instruction design s a. Explain a single bus structure & an I/O interface for an suitable diagram.  b. What is a bus arbitration. What are its types. Explain us	(A) Single Bus (C) Star Bus (B) Multiple Bus (C) Star Bus (D) Ram Bus  i. The advantage of DMA is (A) Avoiding "busy waiting" by CPU (B) High- Speed data transfer between memory & I/O (C) Polling (D) None of these  j. Few addressing modes and fixed instruction size are the features of (A) CISC (B) RISC (C) RAID (D) None of these  Answer any FIVE Questions out of EIGHT Questions.  Each question carries 16 marks.  a. What are the functional elements of a computer? Explain in detail.  b. A computer spends 82% of its time in computing & 18% waiting for the disk The instruction mix and the average cycle per instruction (CPI) for each type is:  Type Instruction% CPI Int 40% I Floating Type 30% 5 Other 30% 5 Considering following 3 modification to the system, calculate speed up for each: (i) The processor is replaced by a new one that reduces the total computation time by 35% (ii) The disc is replaced with a solid state device that reduces the disk waiting time by 85% (iii) The processor is replaced with a new one that has improved floating point performance. The average floating point CPI is reduced to 3, all other aspects are unchanged.  Which modification gives the best speed up?  a. Write the zero and one address instruction for the following expression: X=A*(B-C)/(E+F-G)  b. What is an instruction? Discuss the instruction design set issues.  a. Explain a single bus structure & an I/O interface for an Input device using suitable diagram.  b. What is a bus arbitration. What are its types. Explain using suitable	

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Q.5	a.	What is a serial port? Draw a serial interface.	(3+5)
	b.	What is a PCI bus? What is its use in a computer system? Explain.	(3+5)
Q.6	a.	Analyze the memory hierarchy in terms of speed size and cost.	(8)
	b.	1 0	(3+5)
Q.7	a.	Explain the organization of virtual memory.	(8)
	b.	Explain the organization and accessing of data on a disk.	(8)
Q.8	a.	Explain the working of Booth's algorithm for 7*3.	(8)
	b.	Describe the IEEE754 standard format for single & double precision floating point numbers.	(8)
Q.9	a.	Explain the steps involved in the execution of an instruction.	(8)
	b.	Draw and explain the micro-programmed control unit.	(8)