ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **June 2019** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Noise margin is a measure of circuit's tolerance of
(A) Noise voltage **(B)** signal Voltage
(C) DC Bias **(D)** V_{th}

b. Scan path approach is implemented in
(A) LSSD **(B)** BST
(C) Both **(A)** and **(B)** **(D)** Logical Redundancy

c. The Precharge bus concept limits the following effect
(A) Bus Resistance **(B)** Bus Capacitance
(C) Delay Reduction **(D)** Fast Switching

d. What is the range for LSI?
(A) 10 **(B)** 100-1000
(C) 1000-20000 **(D)** 100000

e. The $Z_{P.U.}/Z_{P.D}$for an inverter driven by an inverter is
(A) 4 **(B)** 2
(C) 8 **(D)** 16

f. Pale Green color in stick encoding scheme represents
(A) Polisilicon-2 **(B)** Polisilicon-1
(C) Via **(D)** Buried Collector

g. DRC at subsystem level is used to check
(A) Correct Wiring up of Leaf Cells
(B) Correct Butting
(C) Both **(A)** and **(B)**
(D) Correct mask making

h. What likely is to happen when Analog and Digital signal lines go in close proximity?
(A) Cross Talk **(B)** No Cross Talk
(C) V_{th} Increases **(D)** More Reliable

i. Which model is suitable to represent a "stuck-at" fault?
(A) Mathematical model **(B)** Physical Model
(C) Logical Model **(D)** None of these

j. Which one is suitable for Testability?
(A) Controllability **(B)** Legibility
(C) Reliability **(D)** Availability

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Determine $Z_{P.U.}/Z_{P.D.}$ for an nMOS inverter driven through one pass transistor. **(6)**

b. Explain all types of encoding schemes for nMOS, CMOS and BiCMOS devices in a tabular form. **(10)**

Q.3 a. Discuss the logical approach to drive a load in BiCMOS inverter design. **(4)**

b. In an nMOS transistor operating at room temperature following measurements are done **(8)**
V_{GS}=4V V_{SB}=2.6V V_{DS}=4V I_D=144μA and the process parameters are W/L=1, t_{ox}=400Å, $|2\Phi_F|$ = 0.64 V & $N_A=10^{16}/cm^3$
Find V_{th}, electron mobility and body effect coefficient. Assume oxide charge Q_{OX}=0

c. For an enhancement type MOS transistor the following parameters were measured. **(4)**
V_{T0} = 0.8V, $\gamma = 0.2V^{1/2}$, $|2\Phi_F|$=0.84V, K´=20μA/V^2, V_{GS}=2.8 V, V_{DS}=5V, V_{BS}= 0V & I_D=0.24mA. Find W/L.

Q.4 a. Discuss advantages of Layout and Design rules. **(4)**

b. Explain lambda- based design rules for nMOS, pMOS and CMOS transistors. **(8)**

c. Draw stick diagrams (nMOS and CMOS) for 2-input NAND gate. **(4)**

Q.5 a. Discuss Rise and fall time factors for a CMOS inverter. **(6)**

b. Discuss Parity generator using basic one-bit cell. Also draw suitable stick diagrams. **(6)**

c. Explain how super buffers are helpful in delay reduction. **(4)**

Q.6 Discuss limitations of scaling in details. **(16)**

Q.7 a. Explain Pseudo-nMOS and Dynamic logics in detail. **(12)**

b. Discuss the concept of Manchester carry-chain. **(4)**

Q.8 a. What is a carry look ahead adder? Discuss Optimization techniques for such an adder. (**10)**

b. Discuss the design of a pseudo-static RAM cell. **(6)**

Q.9 a. Explain Built-In-Self-Test. **(8)**

b. Discuss various CAD Tools for Design and Simulations. **(8)**