ROLL NO. _____

**Code: AE68/AE117** **Subject: EMBEDDED SYSTEMS DESIGN**

# AMIETE – ET(Current & New Scheme)

**Time: 3 Hours** **June 2019** **Max. Marks: 100**

***PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.***

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or the best alternative in the following (2×10)**

a. The design of a particular disk drive has an NRE cost of $100,000 and a unit cost of $20. How much will we have to add to the cost of the product to cover our NRE cost, assuming we sell 4000 units.
**(A)** $20 **(B)** $25
**(C)** $40 **(D)** $50

b. Which design activity is in charge of mapping operations to hardware?
**(A)** Scheduling **(B)** high-level transformation
**(C)** hardware/software partitioning **(D)** compilation

c. Datapath of general-purpose processors consists of ALU and
**(A)** Program counter (PC) **(B)** Instruction register (IR)
**(C)** Registers **(D)** Memory

d. Which of the following has programmable hardware?
**(A)** Microcontroller **(B)** Microprocessor
**(C)** Coprocessor **(D)** FPGA

e. A particular motor operates at 10 revolutions per second when its controlling input voltage is 3.7 V. Assume that you are using a microcontroller with a PWM whose output port can be set high (5 V) or low (0 V). What should be the duty cycle of PWM to obtain 10 revolutions per second.
**(A)** 72 % **(B)** 74 %
**(C)** 76 % **(D)** 78 %

f. In which memory, the signals are multiplexed?
**(A)** DRAM **(B)** SRAM
**(C)** EPROM **(D)** EEPROM

g. Which of the following is used for supporting the priority scheme?
**(A)** Address transfer mode **(B)** Arbitration
**(C)** Counter **(D)** Timer

h. Hard real time operating system has ___ jitter than a soft real time operating system.
**(A)** less **(B)** more
**(C)** equal **(D)** None of these

i. Time required to synchronous switch from the context of one thread to the context of another thread is called
**(A)** threads fly-back time **(B)** jitter
**(C)** context switch time **(D)** None of these

j. Real time systems must have :
**(A)** preemptive kernels
**(B)** non preemptive kernels
**(C)** preemptive kernels or non preemptive kernels
**(D)** neither preemptive nor non preemptive kernels

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2** a. Create a general equation for product cost as a function of unit cost, NRE cost, and number of units, assuming we distribute NRE cost equally among units. Create a graph with the x-axis the number of units and the y-axis the product cost, and then plot the product cost function for an NRE of $50,000 and a unit cost of $5. **(8)**

b. Give an example of a recent consumer product whose prime market window was only about one year. **(8)**

**Q.3** a. Design a 3-bit counter that counts the following sequence: 1, 2, 4, 5, 7, 1, 2, ...,. This counter has an output "odd" that is one when the current count value is odd. Use the sequential design technique. Start from a state diagram, draw the state table, minimize logic, and draw the final circuit. **(6)**

b. Design a custom single-purpose processor implementing the following program. Start with a complex state diagram, construct a datapath and a simplified state diagram, and draw the truth table for the controller, but do not complete the design for the controller beyond the truth table.

```
input_port U;
int V;
for (int i=0; i<32; i++)
V = V + U*V;
```

**(10)**

**Q.4** a. Write an assembly language program of a low-level driver, showing how the parallel port of an x86 based PC performs digital I/O. **(8)**

b. Describe why a general-purpose processor could cost less than a single-purpose processor you design yourself. **(4)**

c. Illustrate how program and data memory fetches can be overlapped in a Harvard architecture. **(4)**

**Q.5** a. Show how to use a 1k x 8 ROM to implement a 512 x 6 ROM. **(8)**

b. Describe how can we interface 8K of data and 32 K of program code memory to a micro-controller, specifically the Intel 8051. **(8)**

**Q.6** a. Describe with details, how 2M bit synchronous pipelined burst SRAM memory device can be interfaced with 32 bit processors. **(8)**

b. Draw a block diagram of a processor, memory, peripheral, and DMA controller connected with a ·system bus, in which the peripheral transfers 100 bytes of data to the memory using DMA. Show all relevant control and data lines of the bus, and label component inputs/outputs clearly. Draw a timing diagram showing what happens during the transfer; skip the 2nd through 99th bytes. **(8)**

**Q.7** a. Suppose that we have a set of 4 tasks. Arrival times Ai , deadlines di and execution times ci are as follows:

T1 : A1 =10, d1 =18, c1 =4
T2 : A2 =0, d2 =28, c2 =12
T3 : A3 =6, d3 =17, c3 =3
T4 : A4 =3, d4 =13, c4 =6

Generate a graphical representation of schedules for this task set, using Earliest Deadline First (EDF) and Least Laxity (LL) scheduling algorithms! For LL scheduling, indicate laxities for all tasks at all context switch times. Will any task miss its deadline? **(8)**

b. Suppose that we have a system comprising two tasks. Task 1 has a period of 5 and execution time of 2. The second task has a period of 7 and an execution time of 4. Let the deadlines be equal to the periods.
Assume that we are using Rate Monotonic Scheduling (RMS). Could any of the two tasks miss its deadline, due to a too high processor utilization? Compute this utilization and compare it to a bound which would guarantee schedulability! Generate a graphical representation of the resulting schedule! Suppose that tasks will always run to their completion, even if they missed their deadline. **(8)**

**Q.8** a. Describe shared-data problem and reentrancy in details. **(8)**

b. What are the different problems in semaphore implementations. Describe about different variants of semaphore. **(8)**

**Q.9** a. For each of the following situations, discuss which of the three shared-data protection mechanism seems most likely to be best and explain why.
(i) Task M and Task N share an *int array,* and each often must update many elements in the array.
(ii) Task P shares a single *char* variable with one of the interrupt routines. **(8)**

b. Discuss about the interrupt routines in an RTOS environment. **(8)**