ROLL NO. _____

Code: AE54/AC54/AT54/AE104
Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT (Current & New Scheme)

Time: 3 Hours **June 2019** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which is sequential circuit?
(A) Mux **(B)** Decoder
(C) Encoder **(D)** Counter

b. 10^3 components are found in _____ ICs.
(A) SSI **(B)** MSI
(C) LSI **(D)** VLSI

c. Which is active device?
(A) Resistor **(B)** Capacitor
(C) Inductor **(D)** Transistor

d. Which is Universal Gate?
(A) NAND **(B)** AND
(C) OR **(D)** XOR

e. In amplifier circuit Gain & Bandwidth is
(A) Proportional **(B)** Inversely Proportional
(C) None of these **(D)** Any of these

f. The number of Flip-Flop required for modulo 9 counter is
(A) 4 **(B)** 5
(C) 6 **(D)** None of these

g. The slew rate of ideal op-amp is
(A) Zero **(B)** Infinite
(C) None of these **(D)** Any of these

h. Which is SOP expression?
(A) $A \cdot B + \overline{A} \cdot \overline{B}$ **(B)** $(A + B)(A + \overline{B})$
(C) A **(D)** None of these

i. The number of 2-input NAND gates required for 2-input XOR gate are
(A) 3 **(B)** 4
(C) 5 **(D)** None of these

j. In half adder circuit P,Q are inputs then carry will be
(A) P AND Q **(B)** P OR Q
(C) P NAND Q **(D)** P NOR Q

PART - A
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Demonstrate different steps of IC fabrication. **(8)**

b. Design the circuit for Ideal Op-Amp. Explain its open-loop operation as well with Feedback. **(8)**

Q.3 a. Explain V to I and I to V converter using Op-Amp. **(8)**

b. Demonstrate Op-Amp as Integrator with its frequency response curve. **(8)**

Q.4 a. Design the Operational Amplifier Circuit and demonstrate all the AC, DC characteristics of Op-Amp circuit. **(8)**

b. Design the Op-Amp as Comparator Circuit and show the mathematical expression and demonstrate the output responses. **(8)**

Q.5 a. Demonstrate 555 timer in monostable mode and explain its operations. **(8)**

b. Explain any one technique for A/D conversion. **(8)**

PART - B
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. What is the difference between Parallel and Serial Transmission of data? Explain. **(6)**

b. Draw and demonstrate all basic gates using universal gates. **(10)**

Q.7 a. Design Full adder circuit using Universal Gates and show the algebraic expression. **(8)**

b. Design BCD adder circuit and show the algebraic expression **(8)**

Q.8 a. Design modulo 13 counters. **(8)**

b. Design SIPO, PISO Shift registers and explain entire function **(8)**

Q.9 a. Define the De Morgan's Theorem with suitable examples. **(8)**

b. Find the minimal-cost circuit for the function **(8)**
$f(x1---x4) = \sum m(0,4,5,12,13,15)$
Assume that the input variables are available in un-complimented form only.