ROLL NO. _____

**Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION**

# AMIETE – CS/IT (Current & New Scheme)

**Time: 3 Hours** **June 2019** **Max. Marks: 100**

***PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.***

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or the best alternative in the following: (2×10)**

a. What is the name of architecture which has separated data & instruction bus

**(A)** Von Neumann **(B)** Harward
**(C)** Both **(A)** and **(B)** **(D)** None of these

b. Functional sequence of CPU since Reset is

**(A)** Fetch- Execute- Decode **(B)** Fetch- Decode – Execute
**(C)** Execute- Fetch – Decode **(D)** Decode – Decode – Execute

c. Instruction AND is executed by

**(A)** Decode unit **(B)** ALU
**(C)** Memory **(D)** Control Unit

d. The sign magnitude representation for +7 is

**(A)** 00001000 **(B)** 10000101
**(C)** 10000111 **(D)** 00000111

e. An example for logical instruction is

**(A)** ADD **(B)** ROTATE
**(C)** INPUT **(D)** MOVE

f. The memory access time is minimized by having

**(A)** Multilevel caches **(B)** Split caches
**(C)** Neither of these **(D)** Both **(A)** and **(B)**

g. Memory- mapped I/O means

**(A)** Using separate memory address space for I/O ports
**(B)** Assigning a part of the main memory address space to I/O ports
**(C)** Using separate input and output instructions
**(D)** None of these

h. On receipt of interrupt, control is transferred to

**(A)** Interrupt vector **(B)** Soft Interrupt
**(C)** Interrupt Service Routine **(D)** None of these

i. If the result of an arithmetic operation does not fit in the range of values, we say _____exception has occurred.

**(A)** Divide by zero **(B)** Invalid
**(C)** Inexact **(D)** Arithmetic

j. Which of the following is not a control instruction?

**(A)** Data Transfer **(B)** Unconditional Jump
**(C)** Function Call **(D)** Procedure Return

**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

**Q.2** a. With a neat diagram explain the Internal organization of a processor. **(8)**

b. What are the important elements of bus design? Show with a labeled diagram the timing of asynchronous bus operation. **(8)**

**Q.3** a. Enlist & explain various types of read only memories. **(8)**

b. What do you mean by instruction cycle and interrupt cycle? Draw the flow chart for interrupt cycle. **(8)**

**Q.4** a. What are addressing modes? Explain the various addressing modes with examples. **(8)**

b. What is Input- Output Interface? Draw and explain block diagram of Input-Output Interface. **(8)**

**Q.5** a. Explain the Concept of Virtual memory. **(8)**

b. How is an overflow detected in Binary Subtraction? What does the overflow signify? **(8)**

**Q.6** a. Draw & explain a general 8-bit parallel interface. **(8)**

b. Multiply $(-9)_{10}$ in binary and $(3)_{10}$ in binary using Booth's algorithm. Also draw the flow chart for floating point multiplication. **(8)**

**Q.7** a. Explain the advantages and disadvantage of Hardwired control. **(8)**

b. Explain interrupt hardware. Elaborate enabling & disabling of interrupts. Use suitable diagram. **(8)**

**Q.8** a. Explain the IEEE floating point number representation in computer with an example. **(8)**

b. Explain DMA. Elaborate the role of Registers & DMA controllers using suitable diagram. **(8)**

**Q.9** a. What is the benefits of using a multiple Bus Architecture compared to single bus Architecture. **(8)**

b. What are the mapping techniques used in Caches. Explain any one technique in detail. **(8)**