

AMIETE - CS/IT {NEW SCHEME}

Time: 3 Hours

June 2019

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

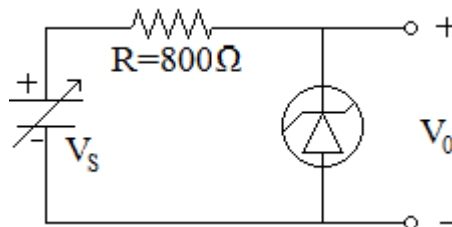
- The open loop gain of an amplifier is 200. If negative feedback with $\beta=0.2$ is used, the closed loop gain will be
(A) 200 (B) 40.12
(C) 4.878 (D) 2.2
- The theoretical maximum efficiency of a half wave diode rectifier is
(A) 40.6% (B) 50%
(C) 81.2% (D) slightly less than 100%
- In CE amplifier circuit, voltage gain is directly proportional to
(A) β (B) collector supply voltage
(C) base resistance (D) None of these
- A Colpitt's oscillator uses
(A) a tapped inductor (B) an inductor & two capacitors
(C) Both (A) and (B) (D) Either (A) or (B)
- If the midband gain of an amplifier is 40 dB the gain at half power frequency is
(A) 37 dB (B) 30 dB
(C) 20 dB (D) 13dB
- In a 4 input AND gate, the total number of high outputs for 16 input states are
(A) 16 (B) 8
(C) 4 (D) 1
- In a four variable k-map, 8 adjacent cells give a
(A) 2 variable term (B) single variable term
(C) 3 variable term (D) 4 variable term

- h. Parallel adder is
 (A) sequential circuit (B) combinational circuit
 (C) Either (A) or (B) (D) None of these
- i. A 4:1 MUX requires _____ data select line.
 (A) 1 (B) 2
 (C) 3 (D) 4
- j. In a positive edge triggered JK FF $J=1, K=0$ and clock pulse is rising Q will be
 (A) 0 (B) 1
 (C) No change (D) Toggle

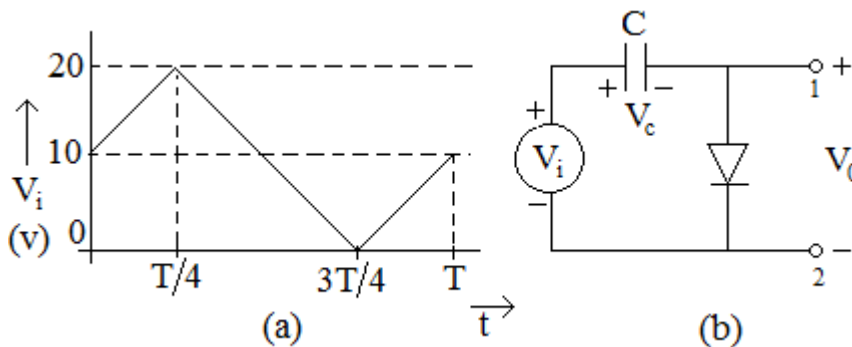
PART A

Answer at least TWO questions. Each question carries 16 marks.

- Q.2** a. Draw the dc equivalent circuit for a diode and the piecewise linear equivalent circuit. Discuss the application of each. (8)
- b. In the below given circuit the zener diode is non-ideal, having a knee voltage $V_{Z0}=9V$ and a dynamic resistance $r_z = 5\Omega$. If the supply voltage V_S varies from 15 to 30 V, determine the range of variation of the output voltage V_0 , also comment on the result. (8)

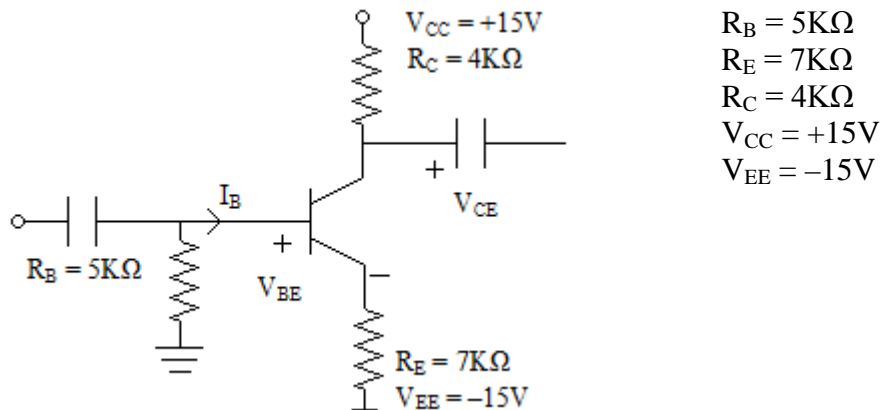


- Q.3** a. Draw the circuit diagram of a basic clamper circuit and explain the operation briefly along with suitable waveforms. (8)
- b. The voltage waveform V_i of Figure (a) is applied to the input of the circuit of Figure (b), Show the output V_0 waveform and mark the voltage levels. Find the PIV of the diode, assumed to be ideal. (8)



- Q.4** a. Explain BJT common-emitter configuration and draw a circuit for determining common-emitter characteristics. (8)

- b. In the circuit of figure shown below $\beta = 99$ and $V_{BE} = 0.7$ V. Calculate the quiescent values of I_B , I_C , I_E & V_{CE} . (8)



- Q.5 a. For a voltage series feedback amplifier, find expression for input and output resistance. (8)
- b. Sketch the circuit diagram of Hartley oscillator and explain its working in detail. (8)

PART - B

Answer at least TWO questions. Each question carries 16 marks.

- Q.6 a. Find the 11's complement of following numbers: (4)
- (i) $(935)_{12}$ (ii) $(267)_{12}$
- b. X and Y are successive digits in positional number system and $(XY)_r = (25)_{10}$ and $(YX)_r = (31)_{10}$. Determine the value of X, Y and r. (4)
- c. Why the Gray code is also known as reflected code? Write a brief note on Gray code and its applications. (8)
- Q.7 a. Minimize the following boolean function using K-Map: (8)
- $$F(A,B,C,D) = \sum m(0,1,2,8,10,11,14,15) \cdot d(9,12)$$
- b. Write a boolean expression for the following state: (8)
- “Z is TRUE if either X or Y is FALSE, otherwise Z is FALSE.” Write a truth table for this expression.
- Q.8 a. How many 3:8 line decoder with enable input are required to construct 6:64 line decoder without using any other logic? Draw its block diagram also. (8)
- b. Implement a full subtractor using two 4:1 Multiplexer. (8)
- Q.9 a. Explain the procedure for conversion of RS Flip Flop to JK Flip Flop. (5)
- b. What is race around condition? How it can be avoided? (5)
- c. Design a binary counter with following binary sequence using D flip flop: (6)
- 0, 1, 3, 2, 6, 4, 5, 7 & repeat