ROLL NO. _____

Code: DE60/DC68/DE111/DC111
Subject: MICROPROCESSORS & MICROCONTROLLERS

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours | **June 2018** | **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which among the following is not a secondary memory storage device.
(A) Hard disk **(B)** RAM
(C) Floppy disk **(D)** Magnetic tape

b. The examples of High-level languages are
(A) BASIC **(B)** FORTRAN
(C) COBOL **(D)** All of these

c. The range of numbers that can be represented for Sign Magnitude notation
(A) $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$ **(B)** $-(2^{n-1}-1)$ to $+(2^{n-1})$
(C) $-(2^{n-1})$ to $+(2^{n-1}-1)$ **(D)** -2^{n-1} to $+(2^{n-1}-1)$

d. The Instruction MOV r1, r2 occupies _____ in memory.
(A) 2 bytes **(B)** 3 bytes
(C) 1 byte **(D)** 4 bytes

e. The Instruction complement in 8085 has the mnemonic
(A) CMC **(B)** CMA
(C) CMP **(D)** CPL

f. Which of the following register is not accessible to the programmer?
(A) B **(B)** C
(C) W **(D)** D

g. The Interrupt pin having the highest priority is
(A) TRAP **(B)** INTR
(C) RST 7.5 **(D)** RST 6.5

h. Which of the following interrupt is non-vectored interrupt?
(A) TRAP **(B)** INTR
(C) RST 7.5 **(D)** RST 6.5

i. INTEL 8255 supports _____ modes of operation.
(A) 1 **(B)** 2
(C) 3 **(D)** 4

j. INTEL 8279 is a _____
(A) DMA controller **(B)** Programmable Interval Timer
(C) Programmable Interrupt Controller **(D)** Keyboard & Display Controller

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Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the following Data Transfer Group of instructions with examples. **(2×5)**
(i) MVI (ii) LXI
(iii) LDA (iv) XCHG
(v) STA

b. Explain the role of Stack and Stack Pointer in 8085. **(6)**

Q.3 a. Explain the purpose of the following registers in 8085. **(4+3+3)**
(i) Program Counter (ii) Instruction Register
(iii) W & Z registers

b. Draw the architecture of 8085. **(6)**

Q.4 a. Write a program for 8085 to exchange 10 bytes of data stored from location X with 10 bytes of data stored from location Y. Also draw the flowchart. **(10)**

b. Write an 8085 ALP to find the smallest 'N' 1-byte numbers. **(6)**

Q.5 a. Describe the various methods of Parallel Data Transfer schemes. **(10)**

b. Describe the action taken by 8085 when it gets interrupted. **(6)**

Q.6 a. Draw the Internal Architecture of 8255 and explain how 8255 interfaces with I/O devices. **(4+6)**

b. Explain the function of following pins of INTEL 8279. **(6)**
(i) RL_{7-0} (ii) SL_{3-0}

Q.7 a. Describe the functions of the registers available in 8259. **(8)**

b. Draw the functional pin diagram of INTEL 8257 and explain the condition when processor is the MASTER and 8257 is in SLAVE mode. **(3+5)**

Q.8 a. Describe the Synchronous data transmission and data reception with neat diagram. **(5+5)**

b. Explain the function of TxRdy and TxC* pins of 8251. **(6)**

Q.9 a. Describe the Internal Data Memory Organization of 8051. **(8)**

b. Explain the various Addressing modes of 8051 with examples. **(8)**