ROLL NO.

Subject: LOGIC DESIGN

DiplETE – ET/CS (Curent & New Scheme)

Time: 3 Hours

Q.

June 2018

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

1	Choose the correct or the best alternative in the following:				
	 a. Nibble is a group of (A) 8 bits (C) 3 bits 	(B) 4 bits (D) 2 bits			
	b. DeMorgan's first theorem is				
	(A) $\overline{X}.\overline{Y} = \overline{X} + \overline{Y}$	$(\mathbf{B})\overline{\mathbf{X}+\mathbf{Y}}=\overline{\mathbf{X}}.\overline{\mathbf{Y}}$			
	$(\mathbf{C})\overline{X} + \overline{X} = 0$	$(\mathbf{D})\overline{X}.X=0$			
	c. A Karnaugh map with 3 variables has				
	(A) 2 cells	(B) 8 cells			
	(C) 16 cells	(D) 4 cells			
	d. The BCD number for decimal 185 is				
	(A) 111011010	(B) 110001110011			
	(C) 10111001	(D) 000110000101			
	e. The output of a gate is high if all the inputs are high. Then it is a				
	(A) NAND	(B) AND			
	(C) EX-OR	(D) OR			
	f. The number of flip-flops required to implement a divide by 64 is				
	(A) 64	(B) 32			
	(C) 16	(D) 6			
	g. The memory which can be programmed by the user and then cannot be era and reprogrammed is		b		
	(A) ROM	(B) PROM			
	(C) EPROM	(D) EEPROM			

Code: DE58/DC58/DE108/DC108

h. A combinational circuit has (A) only memory elements (B) only non memory elements (C) both memory and non memory elements (D) less memory elements i. Alphanumeric codes are____ (A) Un-weighted codes **(B)** 8-4-2-1 codes (C) Weighted codes (D) None of these j. A shift register which can enter the data into it only one bit at a time, but has all the data bits available as an output is _ (A) Serial In / Serial Out (B) Serial In / Parallel Out (C) Parallel In / Serial Out (D) Parallel In / Parallel Out

Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2	a.	What is a digital system? Explain its advantages and disadvantages over analog systems.	(8)
	b.	Convert the following binary numbers to their equivalent decimal values. (i) (11001) ₂ (ii) (1001.1001) ₂	(4)
	c.	Convert the following decimal numbers to their equivalent binary numbers. (i) $(83)_{10}$ (ii) $(127)_{10}$	(4)
Q.3	a.	Find the simplified complemented expression for the following function $F(A,B,C) = ABC + AB\overline{C} + \overline{AB}C + \overline{A}BC$	(4)
	b.	Why NAND and NOR gates known as universal gates? Draw AND, OR and NOT gates realization using NAND and NOR gates.	(8)
	c.	Simplify the following boolean function using K'Map $F(A,B,C,D) = \sum (0,1,2,4,5,6,8,9,12,13,14)$	(4)
Q.4	a.	Explain the application of Flip-Flop as a Shift Register using D Flip-Flops.	(8)
	b.	Draw the logic diagram of JK Flip Flop and explain its working using truth table.	(8)
Q.5	a.	(i) Perform the addition of +25 to -15 using 2's complement system.	(4)
		System.	(4)
	b.	Write the SOP expressions for the Sum(S) and C_{out} of a full-adder. Use a Karnaugh-map to minimize the expressions and then implement them with inverters and AND-OR logic.	(8)

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Q.6	a.	What is an Asynchronous Counter? Draw the logic diagram of MOD-10 Asynchronous Counter and explain its working with the help of timing diagrams.	(8)
	b.	What is a Synchronous Counter? Draw the logic circuit of Synchronous MOD 16 Down Counter and explain its working with timing waveforms.	(8)
Q.7	a.	What is an encoder? Draw the logic circuit of Decimal to BCD encoder and explain its working.	(8)
	b.	What is Magnitude Comparator? Explain 2-bit Magnitude Comparator with the help of truth table.	(8)
Q.8	a.	Draw the logic diagram for 4-bit Serial-in to Parallel-out Shift Register and explain its working with timing waveforms.	(7)
	b.	Design a Mod-6 Synchronous Counter and draw its designed logic diagram.	(9)
Q.9	a.	Draw and explain the architecture of 16×8 ROM.	(8)
	b.	Explain the reading and writing operations in a DRAM cell.	(8)