ROLL NO. _____

Code: DE56/DE106 **Subject: ANALOG ELECTRONICS**

DipIETE – ET (Current & New Scheme)

Time: 3 Hours **June 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Q2 TO Q8 CAN BE ATTEMPTED BY BOTH CURRENT AND NEW SCHEME STUDENTS.**
- **Q9 HAS BEEN GIVEN INTERNAL OPTIONS FOR CURRENT SCHEME (CODE DE56) AND NEW SCHEME (CODE DE106) STUDENTS.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. In an integrated circuit, the SiO2 layer provides
(A) Electrical connection to the external circuit
(B) Physical strength
(C) Isolation
(D) Conducting path

b. In monolithic ICs, all components are fabricated by the process
(A) Evaporation **(B)** Sputtering
(C) Diffusion **(D)** Oxidation

c. An ideal amplifier is one which
(A) Has infinite voltage gain
(B) Responds only to signals at its input terminals
(C) Has positive feedback
(D) Gives uniform frequency response

d. The output admittance h_o of an ideal transistor connected in *CB* configuration in siemens is
(A) 0 **(B)** $1/r$
(C) $1/\beta r_e$ **(D)** -1

e. A JFET has the disadvantage of
(A) Being noisy
(B) Having small gain-bandwidth product
(C) Possessing positive temperature coefficient
(D) Having low input impedance

f. The circuit efficiency of a class A amplifier can be increased by using
(A) Low dc power input **(B)** Direct coupled load
(C) Low rating transistor **(D)** Transformer coupled load

g. In an inverting amplifier the two input terminals of an ideal OP-AMP are at the same potential because
(A) The two input terminals are directly shorted internally
(B) The input impedance of the OP-AMP is infinite
(C) CMRR is infinite
(D) The open loop gain of the OP-AMP is infinite

h. The OP-AMP comparator circuit uses
(A) Positive feedback **(B)** Negative feedback
(C) Regenerative feedback **(D)** No feedback

i. The Schmitt trigger can be used as
(A) Comparator only **(B)** Square wave generator only
(C) Flip flop only **(D)** All of these

j. An OP-AMP shunt regulator differs from the series regulator in the sense that its control element is connected in
(A) Series with line resistor **(B)** Parallel with line resistor
(C) Parallel with load resistor **(D)** Parallel with input voltage

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw the cross-section of a discrete transistor and an IC transistor. Highlight and explain the differences and hence compare their performance. **(6)**

b. What do you understand by thin and thick film technologies? Describe their relative merits, demerits and applications. **(10)**

Q.3 a. Discuss the purpose of an ac load line for a transistor circuit. State how ac load Lines differ from dc load lines for circuits with bypassed emitter resistors, and for Circuits with capacitor coupled loads? **(8)**

b. The collector to base biased CE circuit shown in Fig. 1 has the following transistor parameters: h_{ie} = 1.3kΩ, h_{fe} = 40, h_{oc} = 1.5 ms, Calculate Z_i, Z_o and A_v. **(8)**

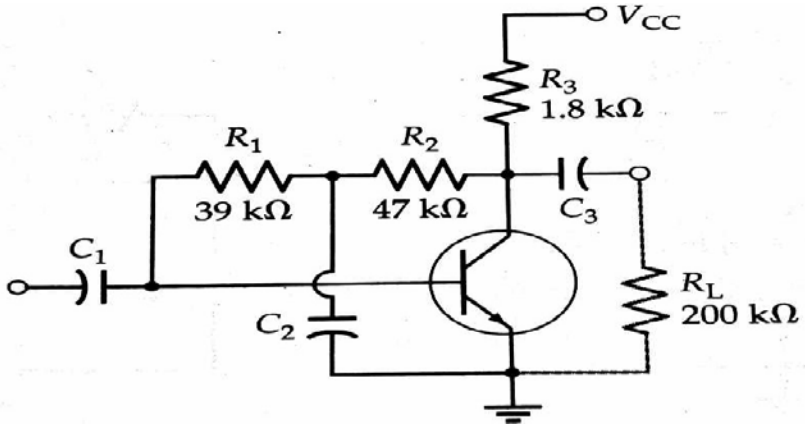

Fig.1

Q.4 a. Draw a diagram of the cross-section of a depletion enhancement mode MOSFET. Identify all parts of the device and explain its operation. **(8)**

b. Sketch a typical JFET switching circuit and explain its operation. Define $r_{DS}(on)$ and $V_{DS}(on)$. **(8)**

Q.5 a. Write equations for a class B transformer coupled amplifier for dc input power to the output stage, ac power delivered to the transformer primary and circuit efficiency. Show that maximum theoretical efficiency of a class B amplifier is 78.6%. **(8)**

b. Draw circuit diagrams to show how a photoconductive cell can be used for
i. Biasing a pnp transistor off when the cell is illuminated
ii. Biasing an npn transistor on when the cell is illuminated
Explain how each circuit operates. **(8)**

Q.6 a. Calculate the output voltage of the circuit shown in Fig. 2 if the input signal is 5.5 mA current. **(8)**

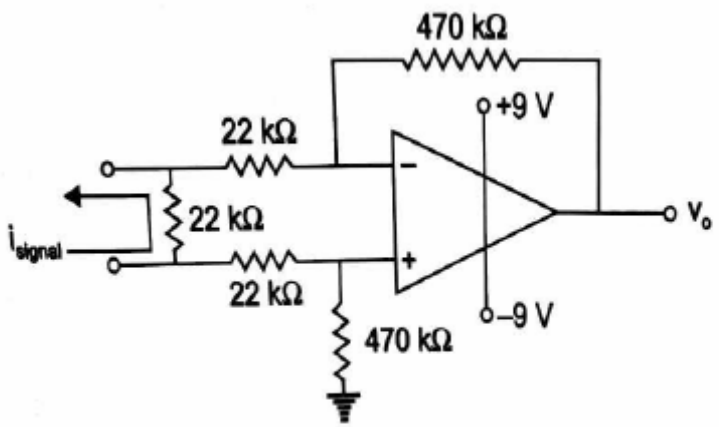

Fig. 2

b In an inverting amplifier $R_1 = 1\,\text{k}\Omega$, $R_f = 100\,\text{k}\Omega$ the OP-AMP has the following specifications: $\frac{\Delta V_{ios}}{\Delta T} = 30\ \mu\text{V/°C max}$, $\frac{\Delta I_{os}}{\Delta T} = 0.3\ \text{nA/°C max}$. Assume that the amplifier is nulled at 25 °C. Calculate the value of the error voltage and the output voltage V_o at 35 °C, if i) $V_i = 1$ mV dc ii) $V_i = 5$ mV dc **(8)**

Q.7 a. Show with the help of a circuit diagram of an OP-AMP used as
(i) scale changer (ii) phase shifter
(iii) inverting adder (iv) non-inverting adder. **(8)**

b Find the transfer function $\frac{v_o}{v_i}$ of the circuit shown in Fig. 3

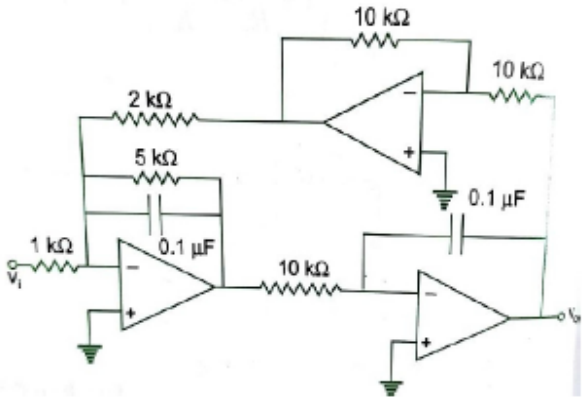

Fig. 3

(8)

Q.8 a. Describe a typical OP-AMP based comparator circuit. Give its types and explain Any one of them in detail. **(8)**

b. The monostable multivibrator shown in Fig. 4 is used as a divide by 3 network. The frequency of the input trigger is 15 KHz. If the value of C = 0.01 µF, calculate the value of resistance R. **(8)**

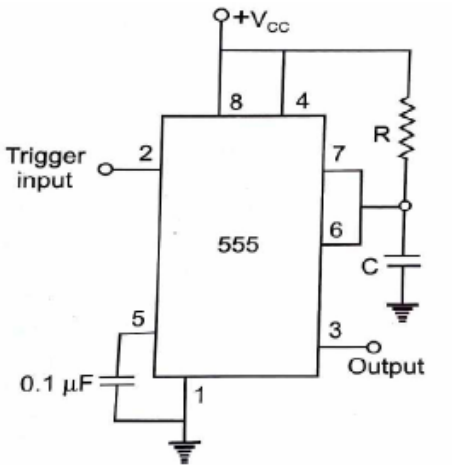

Fig. 4

Q.9 **(For Current Scheme student i.e. DE56)**

a. Draw the schematic of 723 General Purpose Regulator. Describe its operation and explain its various figures of merit. **(8)**

b. Sketch the basic circuit of capacitor coupled class AB complementary symmetry amplifier. Explain the dc biasing and ac operation of the circuit. **(8)**

Q.9 **(For New Scheme student i.e. DE106)**

a. Explain how a solar cell differs from a photodiode. Sketch typical solar cell characteristics and discuss the best operating point on the characteristics. **(8)**

b. Find the voltage at all nodes 0,1,2….. and at the output of a 5 bit R-2R ladder DAC. The LSB bit is 1 and all other bits are equal to 0. Assume V_R = -10V and R=10kΩ. **(8)**