Code: DC57/DC107   **Subject: COMPUTER ORGANIZATION**

DipIETE – CS (Current & New Scheme)

Time: 3 Hours   **June 2018**   **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1   **Choose the correct or the best alternative in the following:**   **(2×10)**

    a. Which memory device is generally made of semi-conductors?
      (A) RAM   **(B)** Hard-disk
      (C) Floppy disk   **(D)** Cd disk

    b. The ALU makes use of _____ to store the intermediate results.
      (A) Accumulators   **(B)** Registers
      (C) Heap   **(D)** Stack

    c. Which registers can interact with the secondary storage?
      (A) MAR   **(B)** PC
      (C) IR   **(D)** R0

    d. CISC stands for _____
      (A) Complete Instruction Sequential Compilation
      (B) Computer Integrated Sequential Compiler
      (C) Complex Instruction Set Computer
      (D) Complex Instruction Sequential Compilation

    e. The Centralised BUS arbitration is similar to _____ interrupt circuit
      (A) Priority   **(B)** Parallel
      (C) Single   **(D)** Daisy chain

    f. When we perform subtraction on -7 and 1 the answer in 2's compliment form is
      (A) 1010   **(B)** 1110
      (C) 0110   **(D)** 1000

    g. Which representation is most efficient to perform arithmetic operations on the numbers?
      (A) Sign-magnitude   **(B)** 1's compliment
      (C) 2'S compliment   **(D)** None of the mentioned

    h. The return address from the interrupt-service routine is stored on the
      (A) System heap   **(B)** Processor register
      (C) Processor stack   **(D)** Memory

    i. The smallest entity of memory is called as _____
       (A) Cell   **(B)** Block
       (C) Instance   **(D)** Unit

    j. The contents of the EPROM are erased by _____
       (A) Overcharging the chip   **(B)** Exposing the chip to UV rays
       (C) Exposing the chip to IR rays   **(D)** Discharging the Chip

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Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q2.   a.   Give the difference between memory address, memory location and byte. **(6)**

       b.   Explain single bus structure. **(5)**

       c.   Explain register transfer notation (RTN). **(5)**

Q3.   a.   Define addressing mode. Explain any four types of addressing mode with example.
                                                                             (2+6)

       b.   Define stack. Explain types of instruction format. **(2+6)**

Q4.   a.   Explain synchronous bus and asynchronous bus. **(8)**

       b   Explain briefly the following: **(2x4)**

         (i) Interrupts   (ii) Direct Memory Access

Q5   a.   Explain serial port and draw a block diagram of a typical serial interface. **(6)**

       b.   Explain the universal serial bus (USB). **(5)**

       c.   How the PCI bus differs from SCSI bus? **(5)**

Q6   a.   Explain static memories and dynamic memories. **(8)**

       b.   What is cache memory? Discuss direct mapping technique. **(8)**

Q7   a.   What do you mean by address translation? Explain a virtual memory address translation based on the concepts of fixed length pages. **(8)**

       b.   Draw the logic circuit of 4-bit carry–look-ahead adder. **(8)**

Q8.   a.   Multiply (-37)*(21), steps of multiplications are to be shown using Booth's algorithm. **(8)**

       b.   Write an algorithm that performs restoring division. **(8)**

Q9.   a.   Describe the following: **(2x4)**
         (i) Hard wired control   (ii) Microprogrammed control

       b.   With the help of figure, explain multiple bus organization. **(8)**