ROLL NO. _____

Code: AE54/AC54/AT54/AE104
Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT (Current & New Scheme)

Time: 3 Hours **JUNE 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. An ideal op-amp is an ideal
(A) voltage controlled current source **(B)** voltage controlled voltage source
(C) current controlled current source **(D)** current controlled voltage source

b. If the differential voltage gain and common mode voltage gain of a differential amplifier are 48 dB and 2 dB respectively, then its common mode rejection ratio is
(A) 23 dB **(B)** 25 db
(C) 46 dB **(D)** 50 dB

c. For a 3 bit R-2R ladder DAC, how many values of resistors are required?
(A) 2 **(B)** 3
(C) 8 **(D)** 1

d. A schmitt trigger exhibits
(A) hysteresis **(B)** amplification
(C) oscillation **(D)** none of these

e. A 555 timer is an IC that can be used to produce
(A) square waves **(B)** triangular waves
(C) sweep waves **(D)** sine waves

f. To derive the compliment of a function, we need to
(A) take dual of a function **(B)** complement each literal
(C) both **(A)** and **(B)** **(D)** none of these

g. $x \oplus y$ means
(A) x but not y **(B)** y but not x
(C) x or y but not both **(D)** neither x nor y but both

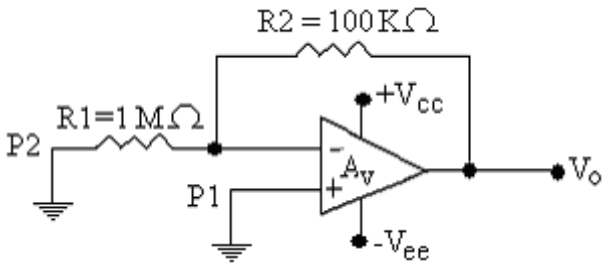
h. The number of input variables which a NOT gate can have is
(A) 1 **(B)** 2
(C) 3 **(D)** Any number

i. The flip-flop which operates in synchronism with external clock pulse is known as ____ flip- flop.
(A) synchronous **(B)** asynchronous
(C) either of the above **(D)** none of the above

j. The number of select lines required for 32:1 multiplexer are ----------
(A) 4 **(B)** 32
(C) 5 **(D)** 8

PART A (Linear ICs)
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Suggest modification in the given circuit of Opamp to make it
(i) inverting (ii) non inverting. **(6)**



b. Discuss the terminal properties of an ideal operational amplifier. **(8)**

c. Show diagrammatically classification of integrated circuits (IC). **(2)**

Q.3 a. Define slew rate. What causes the slew rate? **(4)**

b. Draw and explain the open loop magnitude characteristics for an operational amplifier with single break frequency. **(4)**

c. Draw and explain current to voltage converter circuit using op-amp. **(8)**

Q.4 a. What is an integrator? Derive the formula for its output voltage. Explain its working with neat and clean waveform in case of square wave input. **(10)**

b. Draw and explain Schmitt trigger or squaring circuit. **(6)**

Q.5 a. Draw and explain 3 bit weighted resistor DAC. **(8)**

b. Draw and explain functional diagram of 555 timer IC. **(8)**

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PART B (Digital Electronics)
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. (i) Find decimal equivalent of the binary number $(1\ 1\ 1\ 1\ 1)_2$.
(ii) What do you mean by a memory device? What are the two types of memory devices? **(4)**

b. Make the following conversions. (Steps are necessary)

(i) $(111011)_2$ to octal (ii) $(614)_8$ to decimal
(iii) $(496)_{10}$ to BCD (6)

c. What do you mean by serial and parallel transmission of digital signals? What advantage does parallel have over serial in the transmission of digital signals? **(3)**

d. What do you mean by bit, byte and nibble? **(3)**

Q.7 a. Draw using NAND gate F = A B + ABC + ABCD + ABCD **(5)**

b. Simplify the following:
(i) $A + AB + A\bar{B}$ (ii) (A+B)BC + A **(6)**

c. Minimize the logic function $F(A,B,C) = \sum m(0,4) + d(7,2,1)$ using K-maps. **(5)**

Q.8 a. What is a full adder? Draw truth-table and logic diagram of full adder. **(8)**

b. Add the binary numbers 01101010+00001000+10000001+11111111 **(3)**

c. What is a demultiplexer? How many select lines will be required for an 1:8 demultiplexer? Draw diagram of 1:4 demultiplexer. **(5)**

Q.9 a. Describe NAND gate as a latch. **(8)**

b. Explain the working of 3 bit synchronous counter using J-K F-F and corresponding waveforms. **(8)**