ROLL NO. _____

Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT (Current & New Scheme)

Time: 3 Hours **June 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Floating point representation is used to store
(A) Boolean values **(B)** Whole numbers
(C) Real integer **(D)** Integers

b. The circuit used to store one bit of data is known as
(A) Register **(B)** Encoder
(C) Decoder **(D)** Flip-Flop

c. In computers, subtraction is carried out generally by
(A) 1's complement method **(B)** 2's complements method
(C) Signed magnitude method **(D)** BCD subtraction method.

d. A three input NOR gate gives logic high output only when
(A) One input is high **(B)** One input is low
(C) Two inputs are low **(D)** All inputs are high

e. Cache memory works on the principle of
(A) Locality of data **(B)** Locality of memory
(C) Locality of reference **(D)** Both **(B)** & **(C)**

f. Which of the following is not a control instruction?
(A) Data transfer **(B)** Unconditional jump
(C) Functional call **(D)** Procedural return

g. A virtual memory is one where
(A) Multilevel cache is used
(B) The main memory appears larger than it actually is
(C) A large secondary memory is used
(D) None of these

h. The addressing mode used in an instruction of the form ADD X Y is
(A) Absolute **(B)** Identifier
(C) Index **(D)** None of these

i. What is the name of architecture which has separate data and address memory?
(A) Von Neumann **(B)** Harward
(C) Both **(D)** None of these

j. If arithmetic right shift is performed with 10110101 then result would be
(A) 01011010 **(B)** 11110101
(C) 11011010 **(D)** None

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2	a.	With a top level view describe the different computer components.	**(4)**
	b.	Differentiate between RISC and CISC.	**(6)**
	c.	Write a short note on different generations of computer.	**(6)**
Q.3	a.	Specify the sequence of operations involved when an Instruction is executed.	**(4)**
	b.	Define addressing mode, explain various Addressing Modes with the help of example.	**(6)**
	c.	How Instructions are encoded into 32 bit word? Explain with examples.	**(6)**
Q.4	a.	Distinguish between Memory Mapped I/O and I/O Mapped I/O.	**(4)**
	b.	What is an Interrupt? What are the steps taken when an Interrupt occurs? How the Interrupt is handled occurring exception?	**(6)**
	c.	What is DMA? Explain the block diagram of DMA also describe how DMA is used to transfer data from peripherals.	**(6)**
Q.5	a.	List standard I/O interface	**(4)**
	b.	Write a short note on PCI.	**(6)**
	c.	What are the important elements of Bus Design?	**(6)**
Q.6a.		Analyse the Memory Hierarchy in terms of Speed, Size of Cost.	**(4)**
	b.	What is Mapping Function? What are the ways the Cache can be Mapped?	**(6)**
	c.	Explain LRU replacement algorithm with suitable example.	**(6)**
Q.7a.		Explain Carry look ahead addition using suitable diagram.	**(6)**
	b.	What are RAID Disk Arrays? Explain.	**(4)**
	c.	Explain Virtual-memory address translation with diagram.	**(6)**
Q.8	a.	Multiply using Booth Algorithm 7*3.	**(6)**
	b.	Explain IEEE standard for floating point numbers representation.	**(6)**
	c.	Enlist the rules for Arithmetic operations on Floating point numbers.	**(4)**
Q.9	a.	What is meant by the term Data Path?	**(4)**
	b.	What is the overall function of a Processor's Control Unit?	**(6)**
	c.	Explain the steps involved in execution of a complete instruction.	**(6)**