ROLL NO. _____

Code: AC103/AT103 Subject: ANALOG & DIGITAL ELECTRONICS

AMIETE – CS/IT *{NEW SCHEME}*

Time: 3 Hours **June 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. What causes Gray coding to consume minimum power in instruction fetching from main memory.
(A) High clock frequency **(B)** Longer pipelines
(C) Minimum switching activity **(D)** Large adjacent bit difference

b. Which transistor bias circuit provides good Q-point stability with a single-polarity supply voltage?
(A) Base bias **(B)** Collector-feedback bias
(C) Voltage-divider bias **(D)** Emitter bias

c. Mobility of holes under normal conditions in a silicon diode is given by
(A) $\geq 550\ cm^2\ V^{-1}s^{-1}$ **(B)** $\leq 450\ cm^2\ V^{-1}s^{-1}$
(C) $\geq 650\ cm^2\ V^{-1}s^{-1}$ **(D)** $\geq 1500\ cm^2\ V^{-1}s^{-1}$

d. An NPN transistor is not suitable as a good analog switch because of
(A) Very high input impedance
(B) High reverse gain
(C) Device's asymmetrical dependence on V_{CE} offset
(D) Large transconductance

e. Which method is used to convert a number from an octal base to decimal base?
(A) Direct conversion method **(B)** Decimal equivalent method
(C) Octal equivalent method **(D)** Positional notation method

f. What J-K input condition will always set 'Q' upon the occurrence of the active clock transition?
(A) J = 0, K = 0 **(B)** J = 1, K = 1
(C) J = 1, K = 0 **(D)** J = 0, K = 1

g. The number of states in its counting sequence that a ring counter consisting of 'n' flip-flops can have is
(A) n **(B)** 2^{n-1}
(C) 2^n-1 **(D)** 2^{n+1}

h. A certain multiplexer can switch one of 32 data inputs to its output. How many different Inputs does this MUX have?
(A) 30 data inputs & 5 select inputs **(B)** 32 data inputs and 4 select inputs
(C) 32 data inputs and 5 select inputs **(D)** None of these

i. If a 3-input NOR gate has eight input possibilities, how many of these possibilities will result in a HIGH output?
(A) 1 **(B)** 2
(C) 7 **(D)** 8

j. What should be the applied voltage for a series RLC circuit with I_T = 3 mA, V_L = 30 V, V_C = 18 V, and R = 1000 ohms?
(A) 3.00 V **(B)** 12.37 V
(C) 34.98 V **(D)** 48.00 V

PART-A (ANALOG ELECTRONICS)
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Discuss the doping profile of switching diodes. Do explain the term "reverse recovery time". **(4)**

b. Starting from fundamentals, explain the meaning of the term "SWITCHING TIME" as applied to a Semiconductor diode. What is the use of the above quantity? **(8)**

c. Define 'diffusion capacitance' of a p-n junction diode. Obtain an expression for the same. **(4)**

Q.3 a. Analyze half-wave and full-wave rectifier circuits (without filter) and deduce the expression for its rectification efficiency (assuming ideal diodes). **(8)**

b. Explain the working of Biased Positive Clipper and Biased Negative Clipper circuits. **(8)**

Q.4 a. Explain the switching action of the transistor circuit shown in figure 1 to connect and disconnect a load R_L from the source V_{CC}. **(8)**

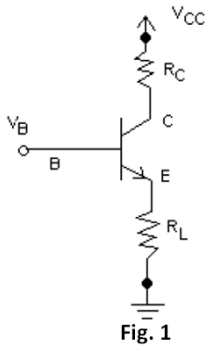

Fig. 1

b. Mention reasons behind the formation of potential barrier in a p-n junction and draw schematic of the junction barrier potential. **(8)**

Q.5 a. Discuss the working principle of a Colpitts oscillator and mention some of its applications. **(8)**

b. In a voltage series feedback amplifier, show that **(8)**
(i) The input impedance increases with negative feedback.
(ii) The output impedance decreases due to negative feedback.

PART-B (DIGITAL ELECTRONICS)
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Draw the logic diagram of a 16-bit ROM Array and explain its working principle. **(8)**

b. Explain the working of a de-multiplexer with the help of an example. **(8)**

Q.7 a. Verify that the following operations are commutative but not associative
(i) NAND (ii) NOR **(8)**

b. Delineate the concept of 'duality' in Boolean algebra. **(8)**

Q.8 a. Design and draw the circuit diagram for a 1 bit digital comparator using basic logic gates to get three different outputs. Also design a four bit comparator using the same circuit. **(8)**

b. List applications of encoder circuits. Draw the schematic of a general encoder with M input and N output. Mention the logic circuit and truth table for an octal-to-binary simple encoder with active-low inputs. **(8)**

Q.9 a. Explain the working of a 4-bit SISO shift register using D-Flip flops and waveforms. **(8)**

b. What is a race around condition in flip-flops? Design a S-R latch using the NOR gates. **(8)**