ROLL NO. _____

Code: DE67/DC67/DE115/DC121 Subject: EMBEDDED SYSTEMS

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Resolution of an n-bit ADC is defined as
(A) $V_{ref}/(2^n)$ **(B)** $V_{in}/(2^n + 1)$
(C) $V_{CC}/(2^n + 1)$ **(D)** $V_{ref}/(2^n - 1)$

b. AND Gate output will be high if two inputs are
(A) 0 0 **(B)** 0 1
(C) 1 1 **(D)** 1 0

c. An embedded system must have
(A) Hard disk **(B)** Processor and Memory
(C) Operating System **(D)** Processor and Input-Output units

d. An embedded system has RAM memory for:
(A) Storing the variables during program run, stack and input or output buffers
(B) Storing all instructions and data
(C) Storing the programs from external secondary memory
(D) Fetching instructions and data into cache(s)

e. Which of the following is an invalid count for BCD counter
(A) 0000 **(B)** 1100
(C) 0101 **(D)** 1000

f. A 40 bit wide address bus can directly access _____ byte of memory
(A) 1K **(B)** 1 Mega
(C) 1 Giga **(D)** 1 Tera

g. In case of UART
(A) UART mode communication is asynchronous and data transfer rate is measured by baud/s
(B) UART mode communication is synchronous, provides start sync code and data transfer rate is measured by baud/s
(C) UART mode communication is synchronous and data transfer rate is measured by bit/s
(D) UART mode communication must provide for parity bit before the stop bit.

h. The function of watch dog timer is
(A) The watchdog Timer is an external timer that resets the system if the software fails to operate properly.
(B) The watchdog Timer is an internal timer that sets the system if the software fails to operate properly.
(C) The watchdog Timer is an internal timer that resets the system if the software fails to operate properly.
(D) None of these

i. The primary job of the operating system is
(A) Manage Commands **(B)** Manage Users
(C) Manage Programs **(D)** Manage Resources

j. In real time operating system
(A) All processes have the same priority
(B) Kernel is not required
(C) A task must be serviced by its deadline period
(D) Process scheduling can be done only once

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Define an embedded system and explain the characteristics of typical embedded systems**.** **(8)**

b. Differentiate between Microprocessors and Microcontrollers. **(8)**

Q.3 a. What is the difference between combinational circuits design and sequential circuits design? **(2)**

b. Explain in detail various steps/procedure involved and practical considerations in designing of Combinational logic circuits. **(6)**

c. Design a Combinational logic circuit using NAND gate only for the following: **(8)**

A circuit has 3-bit input and 1-bit output (Y) specified as follows:
Y = 0, when the input is less than $(5)_{10}$
Y = 1, otherwise

Q.4 a. What is bus explain in context with General Purpose Processor? **(2)**

b. Explain why data bus is bi-directional while address bus is unidirectional? **(4)**

c. A microprocessor has memory chip organized as 64x8, explain how many storage locations it has and what will be the size of Program Counter to access these locations. **(2)**

d. Explain the following: **(8)**
(i) Stack Pointer (ii) Program Counter

(iii) Static and Dynamic RAM (iv) Software and Hardware interrupt

Q.5 a. Explain difference between asynchronous communication and synchronous communication. **(4)**

b. What is meant by communication protocol, draw the frame format of UART protocol? **(4)**

c. Compare RS-232-C and RS422A standards. **(8)**

Q.6 a. Define Direct Memory Access (DMA) and explain its operation in brief. Draw detail interfacing diagram to show interfacing of DMA controller to microprocessor based maximum mode system. **(10)**

b. What is meant by Macros? Discuss advantages and disadvantages of Macros over procedures. **(6)**

Q.7 a. Briefly define each of the following: **(8)**
(i) Cache mapping techniques (ii) Advanced RAM

b. Compose 1K×8 ROMs into an 8K×8 ROM. **(8)**

Q.8 a. What is Real Time Operating System (RTOS)? Discuss major three components of operating systems. **(6)**

b. What is priority inversion and how it is avoided? **(2)**

c. List and elaborate the important parameters to be considered while selecting any RTOS. **(4)**

d. Explain preemptive scheduling method. **(4)**

Q.9 a. Write a short note on Embedded Systems for real time applications. **(6)**

b. Discuss in brief the case study of an embedded system for an adaptive cruise control system in a car. **(10)**