ROLL NO. _____

Code: DC57/DC107 Subject: COMPUTER ORGANIZATION

DipIETE – CS {Current & new Scheme}

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Name the addressing mode in which the effective address is determined by the Index mode using the program counter in place of the general purpose register.
(A) Indirect **(B)** Base-Indexed
(C) Relative **(D)** Auto-decrement

b. The 2's complement representation of (-23) is
(A) 010111 **(B)** 110111
(C) 101000 **(D)** 101001

c. _____ translates a high-level language program into sequence of machine instruction.
(A) Compiler **(B)** Machine translator
(C) Program translator **(D)** Interpreter

d. _____ is an event that causes the execution of one program to be suspended and the execution of another program begins.
(A) Exception **(B)** Interrupt
(C) Subroutine **(D)** Tracker

e. When the I/O devices and the memory space share the same address space, the arrangement is called as _____.
(A) Memory-mapped I/O **(B)** Address controlled I/O
(C) Programmed memory I/O **(D)** Programmed I/O

f. The registers, the ALU, and the interconnecting bus are collectively referred to as the _____.
(A) Datapath **(B)** Subpath
(C) Connecting path **(D)** None of these

g. Zero address instruction format is used for
(A) RISC architecture **(B)** CISC architecture
(C) Von-Neumann architecture **(D)** Stack-organized architecture

h. Arithmetic shift left operation
(A) Produces the same result as obtained with logical shift left operation
(B) Causes the sign bit to remain always unchanged
(C) Needs additional hardware to preserve the sign bit
(D) Is not applicable for signed 2's complement representation

i. The _____ enables the device to recognize its address when the address appears on the address lines.
(A) Interface **(B)** Control circuits
(C) Address decoder **(D)** Data register

j. A 16-bit computer that generates 16-bit addresses is capable of addressing upto _____ memory locations.
(A) 16K **(B)** 64K
(C) 1028K **(D)** 16M

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. With the help of a diagram explain the basic functional units of a computer. **(8)**

b. Convert the following pairs of decimal numbers to 5-bit 2's-complement numbers, and then perform addition and subtraction on each pair. Indicate whether or not overflow occurs for each case. **(4×2)**
(i) 7 and 13 (ii) −12 and 9

Q.3 a. Both of the following statement segments cause the value 300 to be stored in location 1000, but at different times. **(4)**

```
ORIGIN      1000
DATAWORD    300
and  Move   #300, 1000
```

Explain the difference.

b. Elaborate the following terms: **(2×3)**
(i) Two-pass assembler (ii) Loader (iii) Debugger

c. Write a program for adding a list of numbers implemented as a subroutine, LISTADD, with the parameters passed through processor registers. **(6)**

Q.4 a. Discuss DMA approach used to transfer large blocks of data at high speed. **(8)**

b. Discuss handshaking scheme for controlling data transfers on the bus between the master and the slave. Explain the timing of an input data transfer using the handshake scheme. **(8)**

Q.5 a. Draw the block diagram of serial interface and discuss the connection of processor to I/O devices using serial port. **(8)**

b. How the PCI bus is differ from SCSI bus? **(8)**

Q.6 a. Consider a memory consisting of 2M words of 32 bits each. Show how this memory can be implemented using 512K × 8 static memory chips? **(8)**

b. Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 (2K) words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words, which we will view as 4K blocks of 16 words each. With the help of above given data explain the following mapping techniques with proper diagram of cache and main memory: **(4×2)**
(i) Associative Mapping
(ii) Set-Associative Mapping

Q.7 a. What do you mean by address translation? With the help of suitable figure, explain a virtual memory address-translation method based on the concept of fixed-length pages. **(6)**

b. With the help of suitable diagram, explain a circuit that can be used to perform either addition or subtraction of binary numbers. **(6)**

c. Draw the logic circuit of 4-bit carry-look-ahead adder. **(4)**

Q.8 a. With the help of logic circuit arrangement for Binary Division explain Restoring Division algorithm of two unsigned numbers. **(8)**

b. Consider the following 12-bit floating-point number representation format that is manageable for working through numerical exercises. The first bit is the sign of the number. The next five bits represent an excess-15 exponent for the scale factor, which has an implied base of 2. The last six bits represent the fractional part of the mantissa, which has an implied 1 to the left of the binary point. **(8)**
Perform Subtract and Multiply operations on the operands

A	0	10001	011011
B	1	01111	101010

Which represent the numbers

$$A = 1.011011 \times 2^2$$

And

$$B = -1.101010 \times 2^0$$

Q.9 a. Describe the following: **(8)**
(i) Hard-wired control
(ii) Microprogrammed control

b. With the help of figure, explain multiple-bus organization. **(8)**