ROLL NO. _____

Code: CT12 **Subject: COMPUTER ARCHITECTURE**

ALCCS

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. What is meant by overflow in binary addition and how is it detected?

b. What is the difference between restored and non-restored division algorithm?

c. Show using stack operations, how CPU evaluate the notation 45*67*+.

d. Show that any three variable logic function f(x, y, z) can be realized using 2-input multi-plexer. Give the realization & truth table.

e. State how different policies of writing into cache are implemented.

f. Compare DMA based data transfer with program control data transfer.

g. What are zero-address instructions? Explain with the help of an example. **(7×4)**

Q.2 a. What is the philosophy of RISC based machine? How is it different from a CISC Based machine? Discuss briefly. **(4+5)**

b. Derive the equation for speed-up in a parallel computer. Assume your own variables and constants required for derivation. **(9)**

Q.3 a. What is the significance of the addressing modes? Explain the following addressing modes with an example. **(6)**
(i) Implied mode
(ii) Register Indirect Mode
(iii) Indirect Address Mode

b. Discuss RS 232-C standard. State the advantage of USB (Universal Serial Bus) over RS 232-C bus. **(9)**

c. Explain register transfer logic. **(3)**

Q.4 a. The page-address generated by a cache-main memory scheme uses demand paging and has a cache capacity of four pages. Initially the cache was having the pages 1, 2, 3, 4 in it. Which of the page-replacement policies FIFO / LRU is more suitable in this case? Justify by showing the process. **(9)**

b. Explain the following terms:- **(9)**
(i) Transparent mode DMA operation
(ii) Interrupt service routine

Q.5 a. Compare Horizontal Micro Code & Vertical Micro Code. **(6)**

b. Discuss associative mapping technique. **(3)**

c. Explain multiple-module memory interleaving with a block diagram. **(6)**

d. Explain serial data communication. **(3)**

Q.6 a. Differentiate priority interrupt and daisy chain priority interrupt. **(9)**

b. Compare with the help of flowchart/suitable diagram, the difference between micro-programmed control and hard-wired control. **(9)**

Q.7 a. Give Flynn's classification of parallel computer architecture. With the help of diagram discuss each class in brief. **(9)**

b. Design a look ahead carry adder and state its advantages. **(9)**