ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which one of the following is an extra step required in p-well BiCMOS technology?

(A) n+ active area **(B)** active p+ area
(C) p+ buried layer **(D)** n+ buried layer

b. Electron and hole mobility values of a nMOSFET and pMOSFET are 150 cm^2/V-s and 50cm^2/V-s respectively. For a symmetric CMOS inverter design, the ratio between width of nMOSFET and width of pMOSFET is

(A) $\sqrt{3}$ **(B)** $\frac{1}{3}$
(C) $\frac{1}{\sqrt{3}}$ **(D)** 3

c. Latch-up in a CMOS circuit is due to

(A) glitches on supply rail **(B)** incident radiation
(C) parasitic resistors and transistors **(D)** all of these

d. Which of the following statements is false?

(A) two metal layers are parallel to each other
(B) M_0 level is never associated to GND or V_{DD}
(C) more metal layers means large capacitance
(D) all of these

e. If carrier mobility ratio of electrons to holes is four, for equal geometry design, raise time to fall time delay ratio is

(A) 2 **(B)** 4
(C) ½ **(D)** 1/4

f. As a result of scaling, the substrate doping

(A) decreases **(B)** increases
(C) doesn't change **(D)** depends on the type of scaling

g. The maximum possible regularity of an 8×8 bit shifter is

(A) 4 **(B)** 16
(C) 64 **(D)** 256

h. Which of the following is fastest logic style?

(A) CMOS **(B)** pass transistor
(C) domino **(D)** n-p logic

i. In general, increasing area of a gate causes delay to

(A) decrease **(B)** increase
(C) remains constant **(D)** cannot be said

j. Which one of the following is a design fault?

(A) dielectric breakdown **(B)** cross talk
(C) electromigration **(D)** all of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. In a proper sequence, list the main steps involved in a typical n-well process of a CMOS design. **(5)**

b. With neat diagrams, explain important process steps involved in nMOS process. **(9)**

c. What are advantages of enhancement mode MOSFET over depletion mode MOSFET? **(2)**

Q.3 Derive an expression for drain to source current, drain to source current in saturation, saturation drain voltage, transconductance and drain conductance in linear and saturation regions. **(16)**

Q.4 a. What are various rules involved in drawing a stick diagram? **(5)**

b. Explain with an example, various design rules involved in CMOS design. **(5)**

c. Draw stick diagram of a CMOS inverter. **(6)**

Q.5 a. What is meant by sheet resistance? Describe the usage of sheet resistance in CMOS design. **(2)**

b. Estimate rise time and fall time of a CMOS inverter. **(6)**

c. If a CMOS inverter drives a load equal to that of three symmetric inverters, find the rise time and fall time if oxide thickness is 10nm, $|V_{TP}|=V_{TN}=0.4V$, $V_{DD}=1.8V$, $W_n=L_n=180nm$, electron and hole mobility are $150cm^2/V\text{-}s$ and $50cm^2/V\text{-}s$ respectively. **(8)**

Q.6 a. When a MOSFET is scaled down by constant field scaling and constant voltage scaling, how the following device parameters change? **(12)**

Gate delay, saturation current, power dissipation per gate, switching energy per gate, Power speed product, conductor cross section area

b. What are the problems associated with dynamic logic? How the problems with dynamic logic are addressed? **(4)**

Q.7 Draw and design Manchester carry-chain by assuming mobility ratio of two. **(16)**

Q.8 Explain design of a three transistor DRAM cell. How a one transistor DRAM cell performance is compared with a three transistor DRAM cell? **(16)**

Q.9 Explain various techniques employed in testing sequential circuits. **(16)**