ROLL NO. _____

Code: AE68/AE117 Subject: EMBEDDED SYSTEMS DESIGN

AMIETE – ET (Current & New Scheme)

Time: 3 Hours **June 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which one among the following is the fastest form of memory

(A) Random Access Memory (RAM) **(B)** Read only memory (ROM)
(C) Cache memory **(D)** CD ROM

b. An N-bit memory bus can access

(A) N^2 memory locations **(B)** 2^N memory locations
(C) Nx2 memory locations **(D)** 2^N/N memory locations

c. The combinational logic expression C= $A + \bar{A}B$ after reducing becomes

(A) A+B **(B)** A
(C) B **(D)** Can't be reduced further

d. What is the function of watchdog timer?

(A) The watchdog Timer is an external timer that resets the system if the software fails to operate properly.
(B) The watchdog Timer is an internal timer that sets the system if the software fails to operate properly.
(C) The watchdog Timer is an internal timer that resets the system if the software fails to operate properly
(D) None of these

e. In rate monotonic scheduling

(A) shorter duration job has higher priority
(B) longer duration job has higher priority
(C) priority does not depend on the duration of the job
(D) None of these

f. In a vectored interrupt

(A) the branch address is assigned to a fixed location in memory
(B) the interrupting source supplies the branch information to the processor through an interrupt vector
(C) the branch address is obtained from a register in the processor
(D) None of these

g. What will be the affect of following instructions on PSW of 8051
MOV A, #38H
ADD A, #2FH

(A) CY=0, AC=1, P=1 **(B)** CY=0, AC=1, P=0
(C) CY=1, AC=0, P=1 **(D)** CY=1, AC=1, P=0

h. VLIW stands for

(A) Very Large Instruction Word **(B)** Very Long Instruction Word
(C) Very Large Instruction Write **(D)** Very Large Input Words

i. The pipelining process is also called as _____

(A) Superscalar operation **(B)** Assembly line operation
(C) Von neumann cycle **(D)** None of these

j. The process which has just terminated but has yet to relinquish its resource is called

(A) Suspended process **(B)** Zombie process
(C) Blocked process **(D)** Terminated process

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is embedded system? List and define three main characteristics of embedded systems. **(8)**

b. Given the following three cache designs, find the one with the best performance by calculating the average cost of access. Show all calculations.
(i) 4 Kbyte, 8-way set associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles.
(ii) 8 Kbyte, 4-way set-associative cache with a 4% miss rate; cache hit costs two cycles, cache miss costs 12 cycles.
(iii) 16 Kbyte, 2-way set-associative cache with a 2% miss rate; cache hit costs three cycles, cache miss costs 12 cycles. **(8)**

Q.3 a. Explain the flow of Development environment of Software and hardware for Embedded system design. **(10)**

b. Discuss the factors for selection of DSP processor for Embedded System. **(6)**

Q.4 a. Given a timer structured as in Figure-1(a) and a clock frequency of 10 MHz:

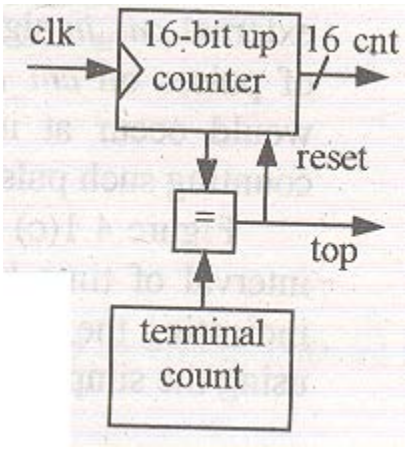

Figure-1(a)

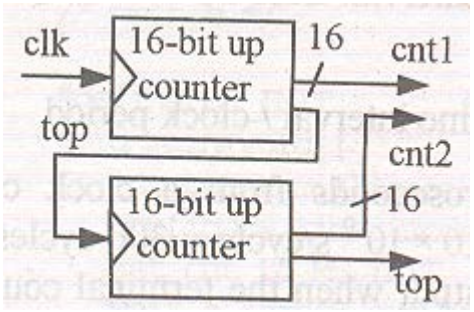

Figure-1(b)

(i) Determine its range and resolution.
(ii) Calculate the terminal count value needed tomeasure 3 ms intervals.
(iii) If a prescaler is added, what is the minimum division needed to measure an interval of 100 ms? (Divisions should be in powers of 2) Determine this design's range and resolution.
(iv) If instead of a prescaler a second 16-bit up-counter is cascaded as in Figure-1(b), what is the range and resolution of this design? **(8)**

b. Write a short note on UART and Watch Dog timer. **(8)**

Q.5 a. Briefly define each of the following: mask-programmed ROM, EPROM, EEPROM, flash EEPROM, RAM, SRAM, DRAM, and NVRAM. **(8)**

b. Discuss the Cache mapping techniques and Cache Replacement Policy in detail. **(8)**

Q.6 a. Explain Peripheral to memory transfer *with* DMA controller. **(10)**

b. Write a Short Note on Controller Area Network (CAN). **(6)**

Q.7 a. When is an RTOS necessary and when is it not necessary in embedded systems? **(8)**

b. Write short notes on the followings:
(i) Pre-emptive and Non pre-emptive task scheduler
(ii) Semaphore **(8)**

Q.8 a. Explain the Memory Management in RTOS For Embedded Systems. **(8)**

b. Write short notes on the followings:
(i) Pipes
(ii) Message Queues
(iii) Shared Memory **(8)**

Q.9 a. What are the rules for interrupt routines in RTOS environment? **(6)**

b. Explain different scheduling algorithms in RTOS. **(10)**