ROLL NO. _____

Code: AE54/AC54/AT54/AE104 **Subject: LINEAR ICs & DIGITAL ELECTRONICS**

AMIETE – ET (Current & New Scheme)

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. An ideal operational amplifier has

(A) Infinite output impedance **(B)** zero input impedance
(C) Infinite bandwidth **(D)** All of these

b. What is the output waveform of the following network?

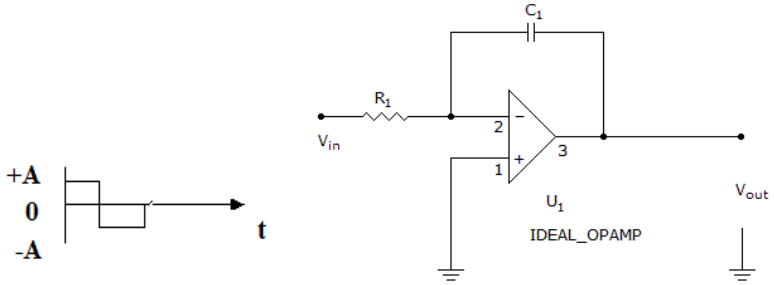

Fig. 1

(A) Sine wave **(B)** Square wave
(C) Triangular wave **(D)** Saw tooth wave

c. What starts a free-running multivibrator?

(A) a trigger **(B)** an input signal
(C) an external circuit **(D)** nothing

d. What will be the binary equivalent of the decimal number 151.75?

(A) 10000111.11 **(B)** 11010011.01
(C) 00111100.00 **(D)** 10010111.11

e. The 555 timer can be used in which of the following configurations?

(A) astable, monostable **(B)** monostable, bistable
(C) astable, toggled **(D)** bistable, tristable

f. When both inputs of a J-K flip-flop reset, the output will:

(A) be invalid **(B)** not change
(C) change **(D)** toggle

g. A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 1010.

(A) 0.3125 V **(B)** 3.125 V
(C) 0.78125 V **(D)** –3.125 V

h. Which of the following expressions is in the sum-of-products (SOP) form?

(A) $Y = (A + B)(C + D)$ **(B)** $Y = AB(CD)$

(C) $Y = AB + \bar{A}B$ **(D)** $Y = (\bar{A} + \bar{B}).(A + B)$

i. A basic S-R flip-flop can be constructed by cross-coupling of which of the basic logic gates?

(A) AND or OR gates **(B)** XOR or XNOR gates
(C) NOR or NAND gates **(D)** AND or NOR gates

j. The Schmitt trigger is a two-state device that is used for:

(A) pulse shaping **(B)** peak detection
(C) input noise rejection **(D)** filtering

PART (A)
Answer at least TWO Questions. Each question carries 16 marks.

Q.2 a. Classify ICs on the basis of application, devices used and chip complexity. **(6)**

b. Calculate the output voltage from the circuit of Fig.2 for an input of 120 μV. **(4)**

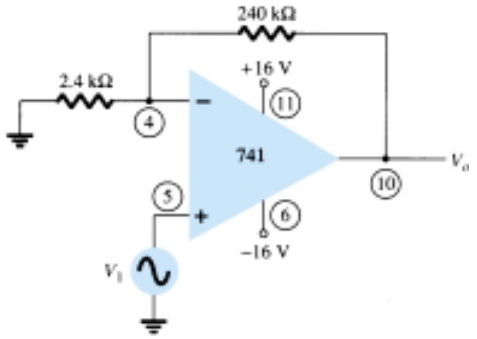

Fig. 2

c. Draw and explain the block diagram of op-amp. Also explain the basic differential amplifier. **(6)**

Q.3 a. For the Instrumentation amplifier as shown in Fig 3. Verify that

$$V_0 = \left[1+\frac{R_2}{R_1}+\frac{2R_2}{R}\right](V_2 - V_1)$$ **(8)**

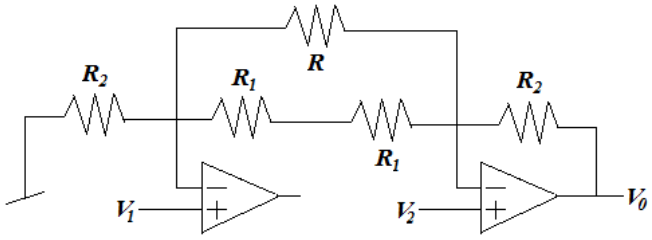

Fig. 3

b. The output of op-Amp Voltage follower is a Triangular wave as shown in Fig.4 for a square wave input of frequency 2MHz and 8 V peak to peak amplitude. What is the slew rate of op-Amp? **(8)**

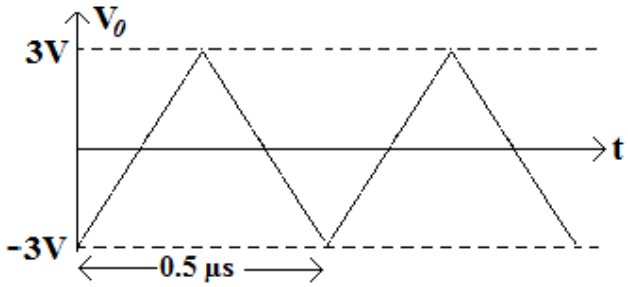

Fig. 4

Q.4 a. Draw a sample and hold circuit. Explain its operation and indicate its uses. **(8)**

b. Explain the following: **(8)**

(i) Transconductance Amplifier
(ii) Schmitt Trigger

Q.5 a. Draw and explain the operation of triangular wave generator. **(8)**

b. What do you understand by DAC techniques? List its various types and explain any one of these. **(8)**

PART (B)

Answer at least TWO Questions. Each question carries 16 marks.

Q.6 a. Explain the following: **(8)**

(i) De Morgan's theorem

(ii) Universal logic gates

(iii) Alphanumeric codes

(iv) Advantages of digital techniques over analog

b. Represent each of the following signed decimal numbers as a signed binary numbers in the 2's complement system. Use a total of five bits, including the sign bit.

(i) +13 (ii) -9 (iii) +3 (iv) -8 **(8)**

Q.7 a. Reduce the combinational logic circuit given in the Fig. 5 to a minimum form. **(6)**

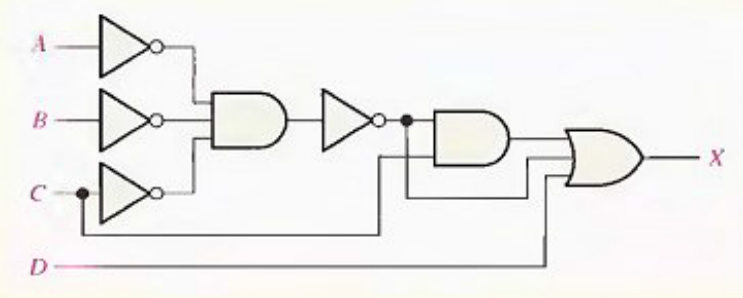

Fig.5

b. Design a logic circuit that has three inputs, A, B, and C and whose output will be HIGH only when a majority of inputs are HIGH. **(4)**

c. Draw K-map and simplify the given expression: **(6)**

f (A,B,C) = AB + A(B + C) + B(B + C)

Q.8 a. Explain the designing of full adder with a neat diagram. **(4)**

b. Implement Full Adder using multiplexers. **(4)**

c. Explain the working of a J-K flip flop? Design DFF using JKFF. **(8)**

Q.9 a. Explain with a neat diagram, the working of synchronous MOD-16 counter. List the advantages of synchronous counters over asynchronous counters. **(8)**

b. Explain **any two** of the following: **(8)**

(i) Ring counter

(ii) D latch

(iii) Serial in parallel out Shift Register

(iv) Propagation delay in Ripple Counter