ROLL NO. _____

Code: AE53/AC53/AT53/AE103
Subject: ELECTRONIC DEVICES & CIRCUITS

AMIETE – ET/CS/IT *{Current & New Scheme}*

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. A loop that does not contain any other loop in it is called
(A) Node **(B)** Branch
(C) Mesh **(D)** Junction

b. In a Half – Wave rectifier with resistive load, the output DC voltage is (Where V_m is peak voltage across transformer secondary)
(A) $\frac{V_m}{\pi}$ **(B)** $\frac{V_m}{2}$
(C) $\frac{V_m}{\sqrt{2}}$ **(D)** $\frac{2V_m}{\pi}$

c. If Emitter - Base junction is reverse biased and Collector – Base junction is forward biased in a BJT, then the device is said to be in
(A) Forward Active **(B)** Saturation
(C) Cut off **(D)** Reverse Active

d. The main advantage of CMOS circuit is
(A) High voltage gain **(B)** Low Power Consumption
(C) Large Current **(D)** Large bandwidth

e. If the individual gains of a two stage RC coupled amplifier are A and B, then the overall gain is equal to (Where A and B are in dB)
(A) A+B **(B)** A-B
(C) A×B **(D)** A/B

f. The maximum theoretical efficiency of series fed class A amplifier is
(A) 50% **(B)** 25%
(C) 78.5% **(D)** 85%

g. The type of feedback configuration in which input impedance decreases and output impedance increases is
(A) Voltage Series **(B)** Voltage Shunt
(C) Current Series **(D)** Current Shunt

h. The frequency of oscillation of Wien Bridge Oscillator is given by

(A) $\frac{1}{2\pi RC}$ **(B)** $2\pi RC$

(C) $\frac{1}{2\pi\sqrt{6}RC}$ **(D)** $2\pi\sqrt{6}RC$

i. The epitaxial growth process is carried out in a reactor at about

(A) $10000^{\circ}C$ **(B)** $5000^{\circ}C$

(C) $1000^{\circ}C$ **(D)** $100^{\circ}C$

j. In class A amplifier, the Q-point, on the load line, lies at

(A) Cut off point **(B)** Centre

(C) Above cut off point **(D)** Beyond cut off point

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. State and explain KCL & KVL. **(8)**

b. Derive the expression for the equivalent resistance when resistances R_1, R_2 *and* R_3 are connected in series and in parallel. **(8)**

Q.3 a. Draw the circuit of Half-wave Rectifier explain its working assuming ideal diode. **(8)**

b. Explain the working of voltage multiplier circuits. **(8)**

Q.4 a. Explain the operating modes of BJT with suitable diagram. **(8)**

b. Calculate the values of I_B, I_C *and* V_{CE} for the circuit shown in Fig.1, if the transistor has β = 100.Assume $V_{BE} = 0.7V$. **(8)**

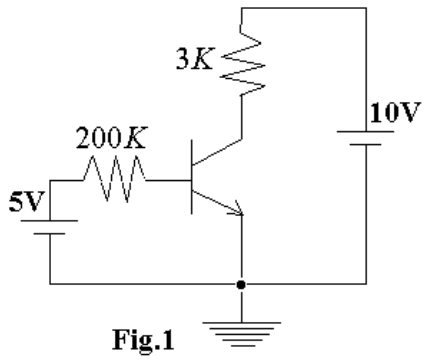

Fig.1

Q.5 a. Explain hybrid Π – model of BJT. **(8)**

b. Explain the circuit of Emitter-Coupled Pair with a neat diagram. **(8)**

Q.6 a. Explain
(i) Frequency distortion (ii) Phase distortion
(iii) Amplitude distortion in amplifier **(9)**

b. Explain the effect of Bypass Capacitor in a BJT amplifier circuit. **(7)**

Q.7 a. Explain the working of a series – fed class A amplifier and derive the expression for its efficiency. **(10)**

b. Explain how the push – pull signals are produced for class B operation. **(6)**

Q.8 a. Explain the effect of negative feedback on
(i) Non linear distortion & noise
(ii) Gain & Bandwidth **(8)**

b. Draw the circuit of UJT Relaxation Oscillator and derive the expression for its frequency of oscillation. **(8)**

Q.9 a. Write the advantages of IC technology. **(4)**

b. Explain the Photolithography process in IC fabrication. **(6)**

c. Explain the PNP transistor fabrication. **(6)**