ROLL NO. _____

Code: AC103/AT103 Subject: ANALOG AND DIGITAL ELECTRONICS

AMIETE – CS/IT (New Scheme)

Time: 3 Hours **JUNE 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. To obtain very high input and output impedances in a feedback amplifier, the topology mostly used is
(A) Voltage-series **(B)** Current-series
(C) Voltage-shunt **(D)** Current-shunt

b. An amplifier has an input signal voltage of 0.054 mV. The output voltage is 12.5 V. The voltage gain in dB is
(A) 53.6 dB **(B)** 107.3 dB
(C) 231 dB **(D)** 116 dB

c. A 6.2 V zener is rated at 1 watt. The maximum safe current the zener can carry is
(A) 1.61 mA **(B)** 161 mA
(C) 16.1 mA **(D)** 0.61 mA

d. An amplifier has an output voltage of 7.6 V p-p at the midpoint of the frequency range. What is the output at f_c?
(A) 3.8 V p-p **(B)** 3.8 V_{rms}
(C) 5.4 V_{rms} **(D)** 5.4 V p-p

e. Rectification efficiency of a full wave rectifier without filter is nearly equal to
(A) 51% **(B)** 61%
(C) 71% **(D)** 81%

f. The frequency of oscillation of a tunnel-collector oscillator having L= 30μH and C = 300pf is nearby
(A) 267 kHz **(B)** 1677 kHz
(C) 1.68 kHz **(D)** 2.67 MHz

g. If the output voltage of a bridge rectifier is 100V, the PIV of diode will be
(A) $100\sqrt{2}$V **(B)** $200/\pi$ V
(C) 100π V **(D)** $100\pi/2$ V

h. The main advantage of a crystal oscillator is that its output is
(A) 50Hz to 60Hz **(B)** Variable frequency
(C) A constant frequency **(D)** D.C.

i. The lowest output impedance is obtained in case of BJT amplifiers for
(A) CB configuration **(B)** CE configuration
(C) CC configuration **(D)** CE with R configuration

j. The POS form of logical expression is most suitable for designing logic circuits using only
(A) XOR gates **(B)** NOR gates
(C) NAND gates **(D)** OR gates

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the difference in Conductors, Insulators, and Semiconductors using the energy band diagram. **(5)**

b. Derive mathematical expression for Fermi Dirac- Probability function. **(5)**

c. A diode current is 0.6mA when the applied voltage is 400mV, and 20mA when the applied voltage is 500mV. Determine η. Assume $\frac{KT}{q} = 25\text{mV}$. **(6)**

Q.3 a. In a centretap fullwave rectifier, the load resistance R_L=1KΩ. Each diode has forward biased dynamic resistance r_d of 10Ω.The voltage across half the secondary winding is $220\sin 314t$. Find **(5)**
(i) The peak value of current.
(ii) The DC or Average value of current.
(iii) The RMS value of current.
(iv) The ripple factor and
(v) The rectification efficiency.

b. Draw and explain Zenor diode as a voltage regulator. **(5)**

c. Design a positive clipper and series and shunt circuits and explain input and output signal waveforms. **(6)**

Q.4 a. Design a basic transistor amplifier in common base configuration and explain its amplification action with suitable example. **(8)**

b. For a emitter biased circuit, V_{CC} = +10V, R_C = 1.5KΩ, R_B = 270Ω and R_E = 1kΩ, Assuming β = 50, Determine. **(8)**
(i) Stability factor (ii) I_B (iii) V_{CE} (iv) V_C
(v) V_E (vi) V_B (vii) V_{BC}

Q.5 a. Design a transistor based voltage divider biasing circuit and use same circuit into an amplifier. Also explain function of coupling capacitor and bypass capacitor. **(8)**

b. Draw the circuit of Hartley Oscillator and explain its working. Derive the expression of frequency of oscillation and condition for starting of oscillation. **(8)**

Q.6 a. Convert the following octal numbers into Decimals:- **(4)**
(i) $(444)_8$ (ii) $(237)_8$

b. Convert $(112)_{10}$ and $(253)_{10}$ to hexadecimal number. **(4)**

c. Explain Parity method for error detection with an example of noise causing an error in the transmission of digital data. **(8)**

Q.7 a. Simplify the expression $Z = \overline{(\overline{A} + C) \cdot (B + \overline{D})}$. **(6)**

b. Design OR, AND, and NOT gate using one of the universal gates. **(5)**

c. Simplify the expression; $x = (\overline{A} + B)(A + B + D)\overline{D}$ **(5)**

Q.8 a. Draw and explain block diagram of a five-bit parallel adder circuit using full adder. **(8)**

b. Design a four input multiplexer and explain its operation with truth table. **(8)**

Q.9 a. Design a clocked J-K flip-flop that respond only to the positive edge of the clock and draw the waveform. **(8)**

b. Design a Synchronous MOD-16 Counter. **(8)**