Code: DC04 **Subject: COMPUTER ORGANISATION**
Time: 3 Hours **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2 ×10)**

a. In a 8086/8088 Microprocessor, the unit responsible for getting the instructions from the memory and loading in the queue is:

(A) Execution Unit **(B)** Registers
(C) Stack **(D)** Bus Interface Unit

b. What characteristic of RAM memory makes it <u>not</u> suitable for permanent storage?

(A) Too slow **(B)** Unreliable
(C) It is volatile **(D)** Too bulky

c. A given memory chip has 12 address pins and 4 data pins. It has the following number of locations.

(A) 2^4 **(B)** 2^{12}
(C) 2^{48} **(D)** 2^{16}

d. A computer that is advertised as having a 96 K byte DRAM memory and a 2.1 Gigabyte hard drive has

(A) 96 K bytes of primary memory and 2.1 Gigabytes of secondary memory
(B) 2.1 Gigabytes of primary memory and 96K bytes of secondary memory
(C) 96 bytes of cache, 2.1 gigabytes of primary memory
(D) 96 K bytes of cache, 96 K bytes of primary memory, and 2.1 Gigabytes of secondary memory

e. Virtually all computer designs are based on the von Neumann architecture. A high level view of this architecture has the following three components:

(A) Buses, memory, input/output controllers
(B) Hard disks, floppy disks, and the CPU
(C) Memory, the CPU, and printers
(D) Memory, input/output modules, and the CPU

f. The ascending order or a data Hierarchy is

(A) bit - bytes - fields - record - file - database
(B) bit - bytes - record - field - file - database
(C) bytes - bit- field - record - file - database
(D) bytes -bit - record - field - file - database

g. Interrupts which are initiated by an I/O drive are

(A) internal **(B)** external
(C) software **(D)** all of above

h. Memory access in RISC architecture is limited to instructions

(A) CALL and RET **(B)** PUSH and POP
(C) STA and LDA **(D)** MOV and JMP

i. Pipelining strategy is called implement

(A) instruction execution **(B)** instruction prefetch
(C) instruction decoding **(D)** instruction manipulation

j. The process of producing results from the data for getting useful information

(A) output **(B)** input
(C) processing **(D)** storage

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain a timing diagram for an example of Register Transfer. **(6)**

b. Simplify the following Boolean Function Using K-Maps:
$F(a,b,c,d)= \sum (0,1,2,3,4,5,7,10,11,15)$. **(6)**

c. Draw a block diagram to illustrate the basic organization of computer system and explain the function of various units. **(4)**

Q.3 a. Draw a neat block diagram of a 4-bit binary adder-subtractor. Then, explain its operation in detail. **(8)**

b. Discuss the utility of RISC and CISC architectures by comparing their various features. Give suitable diagrams also. **(8)**

Q.4 a. What is the need of a control unit in a computer? What is the difference between hardwired control and micro-program control? **(6)**

b. Write an assembly program to reverse a given string. **(6)**

c. What do you mean by pseudo instruction? Explain. **(4)**

Q.5 a. Explain the following addressing modes with one example each. Also give one use of each addressing mode

(i) Register addressing
(ii) Index addressing
(iii) Stack addressing
(iv) Base addressing scheme **(8)**

b. Give an example of the addition of two floating point Operands using an arithmetic pipeline. Show all the steps involved. **(8)**

Q.6 a. What is U A R T? What is baud rate? Consider a serial transmission whose transfer rate is 9 characters per second. The system uses 2 stop bits and has eight signaling states. Calculate its baud rate. **(8)**

b. How is a program executed in computer? List steps associated with each instruction cycle. Explain Fetch and Decode phase. Draw the block diagram of a register transfer for fetch phase. **(8)**

Q.7 a. Draw the flowchart of Booth algorithm for multiplication of signed 2's complement numbers and explain it with an example. **(8)**

b. Perform subtraction with the following unsigned binary numbers by taking the two's complement of the subtrahend. 11010 – 01101. **(8)**

Q.8 a. What is a DMA scheme of Data Transfer? Discuss its operating principle. What is a burst mode of data transfer and cycle stealing mode of data transfer? **(10)**

b. Differentiate between Polling and Interrupt Driven I/O. **(6)**

Q.9 a. An 8-bit micro-processor has a 16-bit address bus. The first 15 lines of the address are used to select Bank of 32 K bytes of memory. The high order bit of the address is used to select a register which receives the contents of a data bus. Explain how this configuration can be used to extend the memory capacity of the system of 8 banks of 32 K bytes for a total of 256 K bytes of memory. **(8)**

b. Describe cache memory organization. Explain the various types of mapping procedures used by cache memory. **(8)**