## AMIETE - ET (NEW SCHEME) - Code: AE68

## **Subject: EMBEDDED SYSTEMS DESIGN**

Time: 3 Hours		Max. Marks: 100
	JUNE 2011	

NOTE: There are 9 Questions in all.

• Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.

<ul> <li>The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.</li> <li>Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.</li> <li>Any required data not explicitly given, may be suitably assumed and stated.</li> </ul>				
Q.1	C	hoose the correct or the b	pest alternative in the following:	(2×10)
	a.	Identify which of these ar	re real-time applications scenarios	
			ing system port of a company's annual report ransactions in an account book of a small compan	у
	b.	Which of the following ar	re commercially claimed RTOS	
		( <b>A</b> ) Linux ( <b>C</b> ) Windows 2000	<ul><li>(B) Windows 7</li><li>(D) Vx works</li></ul>	
	c.	With the pas it would a register	rocessor can read from or write to a port directly	y just
		<ul><li>(A) Port based I/O</li><li>(C) Memory mapped I/O</li></ul>	<ul><li>(B) Bus based I/O</li><li>(D) None of the above</li></ul>	
	d.	Which of the following inversion problem?	strategy is employed for overcoming the pri	iority
			-	·S
	e.	A/an routine n	nust not call any RTOS function that might bloc	k the
		(A) Timer (C) I/O	<ul><li>(B) Serial Communication</li><li>(D) Interrupt</li></ul>	

		<ul><li>(A) In the kernel space</li><li>(B) In the user space</li><li>(C) In separately allocated space which</li><li>(D) Anywhere in free space</li></ul>	ch is neither kernel space nor user space	e			
	g.	For what types of operations is DMA useful?					
		<ul> <li>(A) For large &amp; fast data transfers between memory &amp; I/O devices</li> <li>(B) For large &amp; slow data transfers between memory &amp; I/O devices</li> <li>(C) For slow &amp; small data transfers between memory &amp; I/O devices</li> <li>(D) For small data transfers between memory &amp; cache</li> </ul>					
	h.	When a process is rolled out of memory, it loses its ability to use the CPU (at least for a while). Describe another situation where a process loses its ability to use the CPU, but where the process does not get rolled out.					
		<ul><li>(A) When an interrupt occurs</li><li>(B) When thrashing occurs</li><li>(C) When deadlock occurs</li><li>(D) While swapping</li></ul>					
	i.	Running, ready and block are concerned to					
			<ul><li>(B) Semaphore State</li><li>(D) Pipe State</li></ul>				
	j.	Semaphores and queues arefunction call	so that interface between modules is a	ı			
			(B) Encapsulate				
		(C) Polymorphic	(D) Separate				
Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.							
Q.2	a.	What is an embedded system? Gives sophisticated scale embedded system.	-	& ( <b>8</b> )			
	b.	Explain top-down design process tecl	hnology for Embedded System.	<b>(4)</b>			
	c.	Distinguish between a combinational	circuit and a sequential circuit.	<b>(4)</b>			
Q.3	a.		te functional circuits of a microcontroll dded software in Assembly Language?				
	b.	What is GPP & ASIP?		(4)			

f. Where are the device drivers located in RTOS with a microkernel?

	c.	Explain the Hardware units of an Embedded System? Give advantages of writing embedded software in C Language. (6)	
Q.4	a.	Given a 120-step stepper motor with its own controller, write a C function <i>Rotate (int degrees)</i> , which, given the desired rotation amount in degrees (between 0 and 360), pulses a microcontroller's output port the correct number of times to achieve the desired rotation. (6)	
	b.	Compute the memory needed in bytes to store a 4-bit digital encoding of a 3-second analog audio signal sampled every 10 milliseconds. (4)	
	c.	Explain the synchronous, asynchronous and isosynchronous communication techniques. Give their respective applications. (6)	
Q.5	a.	Explain the following:- (i) PROM (ii) Flash EEPROM (iii) NVRAM	
	b.	Explain ROM image, stack overhead and memory optimization. (6)	
	c.	A given design with cache implemented has a main memory access cost of 20 cycles on a miss and two cycles on a hit. The same design without the cache has a main memory access cost of 16 cycles. Calculate the minimum hit rate of the cache to make the cache implementation worthwhile. (4)	
Q.6	a.	Define protocol. Name any two characteristics to be taken into account while interfacing a device. (4)	
	b.	Define interrupt handler. Explain the difference between port-based I/O and bus-based I/O. (4)	
	c.	Give advantages and disadvantages of using memory-mapped I/O versus standard I/O. (4)	
	d.	Differentiate between parallel, serial and wireless communication. Give two common applications for each. (4)	
Q.7	a.	Differentiate between (9)	
		<ul><li>(i) Recursive and Reentrant function</li><li>(ii) Queue and Stack</li><li>(iii) RTOS and Non-RTOS</li></ul>	
	b.	Define a semaphore and what is shared data problem? Briefly explain the problems that may arise while using semaphores? (7)	
Q.8	a.	Explain the following (i) Message Queue (ii) Mailbox (iii) Pipe	

- b. Explain any two features of RTOS. What are the strategies used by RTOS on interrupt source calls? (6)
- c. What is memory management and how will it influence the real-time behaviour of an operating system? (4)
- **Q.9** a. Define the following:-

**(6)** 

- (i) Inter process communication
- (ii) Soft Real time systems
- (iii) Hard Real time Systems
- b. Differentiate between

(10)

- (i) Kernel space versus user space versus real-time space.
  - (ii) Monolithic kernel versus micro-kernel.