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## AMIETE – ET/CS/IT (NEW SCHEME) - Code: AE54/AC54/AT54

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**Subject: LINEAR ICs & DIGITAL ELECTRONICS**

**Time: 3 Hours**

**Max. Marks: 100**

### JUNE 2011

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

**Q.1 Choose the correct or the best alternative in the following: (2×10)**

- a. The minimum gain required for an op amp so that the error in the gain from the ideal is less than 0.1% when the op amp is used as a voltage follower is \_\_\_\_\_
- (A) 999 (B) 1000  
(C) 1001 (D) 10000
- b. An op amp has a common mode gain of 5, and CMRR of 94dB. If its differential input is 2μV and the common mode input of 1mV, the output in mV is equal to\_\_\_\_\_.
- (A) 495 (B) 500  
(C) 505 (D) 510
- c. The slew rate of an op amp is 3.14 V/μsec. If the frequency of the sinusoidal input to the voltage follower using this op amp is 5 kHz, the maximum amplitude of the input that could be applied so that the output is not distorted is equal to\_\_\_\_\_.
- (A) 31.4 V (B) 50 V  
(C) 62.8 V (D) 100 V
- d. The output voltage in the circuit of Fig.1 is equal to\_\_\_\_\_.

- (A) 0 V  
(B) -1 V  
(C) +1 V  
(D) -4 V

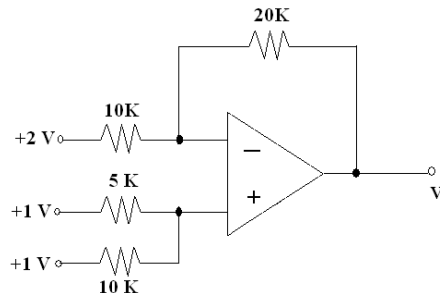
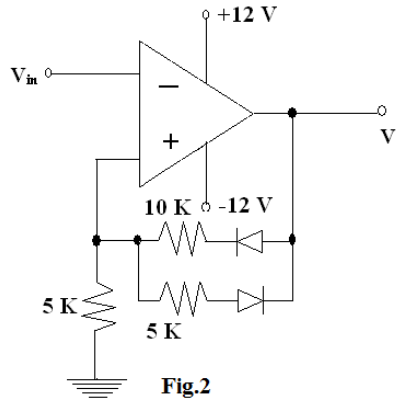


Fig. 1

e. In the Schmitt trigger circuit of Fig.2, the UTP (Upper Trigger Point) is equal to \_\_\_\_\_.

- (A) -6 V
- (B) -4 V
- (C) +4 V
- (D) +6 V



f. The hexadecimal equivalent of the decimal number 4444 is equal to \_\_\_\_\_.

- (A) 115C
- (B) 114D
- (C) C511
- (D) D411

g. The 2-input EXCLUSIVE-OR gate gives HIGH output when both the inputs are \_\_\_\_\_.

- (A) LOW
- (B) HIGH
- (C) Equal
- (D) Different

h. The minimum number of NOR gates required to realize an EXCLUSIVE-OR function (using only NOR gates) is \_\_\_\_\_.

- (A) 3
- (B) 4
- (C) 5
- (D) 6

i. If the input frequency to a ripple counter using 5 flip flops is 1 MHz, the output frequency is equal to \_\_\_\_\_.

- (A) 100 kHz
- (B) 20 kHz
- (C) 3.5 kHz
- (D) 31.25 kHz

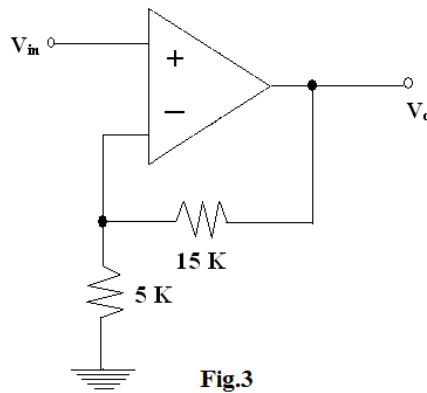
j. The main advantage of parallel comparator A/D converter is

- (A) Accuracy
- (B) Low noise
- (C) Low cost
- (D) Low conversion time

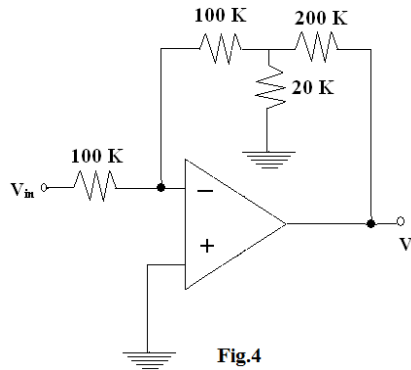
**PART (A)**

**Answer At least TWO questions. Each question carries 16 marks.**

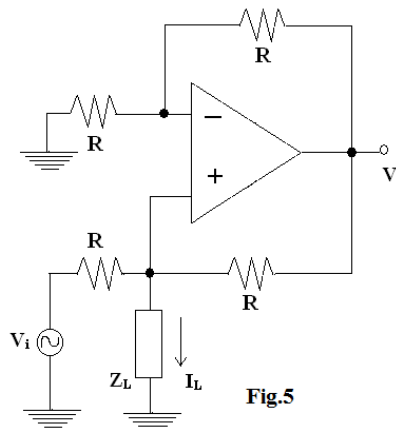
- Q.2** a. In the circuit of Fig.3, determine the voltage gain  $v_o/v_i$  and the input impedance of the non-inverting amplifier. The op amp has an input impedance of 500 K $\Omega$ , output impedance of 500 $\Omega$  and an open loop gain of  $10^4$ . (8)



- b. In the circuit of Fig.4, determine the output voltage if the input voltage is 10mV. Assume that the op-amp is ideal. (8)



- Q.3** a. Design a circuit using two ideal op amps to obtain an output  $V_0 = V_1 - 2V_2 + 3V_3 - 4V_4$ . Inputs available are only  $+V_1, +V_2, +V_3$  and  $+V_4$ . (8)
- b. In the circuit of Fig.5, obtain the expression for  $I_L$ . (8)



- Q.4** a. Draw the circuit of a integrator using an ideal op amp, and prove that it works as an integrator. (5)
- b. What modifications are required to make the circuit in Q.4 (a) a practical integrator circuit. (3)

- c. Design a Schmitt trigger circuit using an ideal op amp operating with +15V and -15V, to have the upper and lower trigger points as +8V and -6V respectively. Also draw the output waveform if the input is a 10V peak sinusoidal signal. (8)

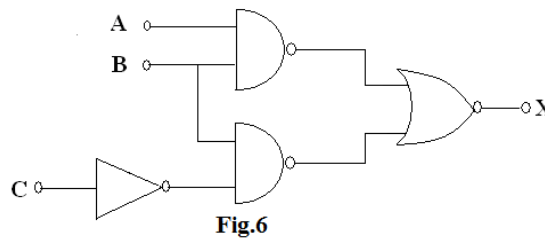
- Q.5** a. With a neat diagram explain the working of an R-2R ladder type D/A converter. What are its main advantages with respect to a weighted resistor D/A converter? (8)
- b. Draw the circuit of a monostable multivibrator using 555 timer IC, and design the values for the different components in the circuit so that the output pulse width is 0.2 msec. (8)

**PART (B)**

**Answer At least TWO questions. Each question carries 16 marks.**

- Q.6** Perform the following conversions: (2×8)
- (i)  $(756.75)_{10} = ( )_2$  (ii)  $(101111.101)_2 = ( )_{10}$  (iii)  $(463.25)_{10} = ( )_8$
- (iv)  $(672.46)_8 = ( )_{10}$  (v)  $(4680.125)_{10} = ( )_{16}$  (vi)  $(9A8E.D)_{16} = ( )_{10}$
- (vii)  $(76EF.AB)_{16} = ( )_8$  (viii)  $(125.75)_8 = ( )_{16}$

- Q.7** a. Implement the given function  $f(A, B, C) = A + BC$  by using  
 (i) NAND gate (ii) NOR gate (5)
- b. Draw the logic circuit to implement the OR function using only NAND gates. (5)
- c. Obtain the logic expression for the output X of the circuit in Fig.6, and simplify it using De Morgan's theorems. (6)



- Q.8** a. Show how a 16 input multiplexer is used to generate the function  
 $f(A, B, C, D) = \overline{A} \overline{B} \overline{C} D + BCD + \overline{A} \overline{B} D + ABCD$  (6)
- b. Draw the truth table for 'DIFFERENCE' and 'BORROW' of a FULL SUBTRACTOR. From the truth table, obtain logic expressions for them. From these expressions realize the FULL SUBTRACTOR using logic gates. (10)
- Q.9** a. Draw the circuit of a latch using two NOR gates and explain its operation. (4)
- b. Draw the internal circuit of an edge triggered D flip-flop and explain its functioning using necessary waveforms. (6)
- c. Draw the circuit of a MOD-60 ripple counter to reduce 60Hz to 1Hz, using JK flip-flops and explain its operation with its state transition diagram. (6)