Code: AE09 **Subject: ANALOG & DIGITAL ELECTRONICS**
Time: 3 Hours **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. If an inverting amplifier has the non inverting pin of the op-amp connected to ground, the inverting pin of the op-amp will be _____.

(A) at ground **(B)** at virtual ground
(C) equal to V_{in} **(D)** equal to V_{out}

b. Slew rate distortion is more prevalent in circuit with _____.

(A) small input voltage swings **(B)** large input voltage swings
(C) small output voltage swings **(D)** large output voltage swings

c. The cut off frequency is also referred to as the _____.

(A) half power point **(B)** low end frequency
(C) higher end frequency **(D)** both **(B)** and **(C)**

d. The network of resistors containing only two values are known as

(A) binary divider **(B)** binary ladder
(C) analog divider **(D)** analog ladder

e. When a transistor switch is in saturation V_{CE} is approximately equal to _____

(A) V_{CC} **(B)** V_B
(C) 0.2V **(D)** 0.8V

f. Which of the following flipflop is used as latch?

(A) JK flipflop **(B)** SR flipflop
(C) D flipflop **(D)** T flipflop

g. TTL totempole output stage is primarily used to

(A) increase the noise margin of the gate
(B) decrease the output switching delay
(C) facilitate a wired OR logic connection
(D) increase the output impedance of the circuit

h. A full adder can be made of

(A) two half adder
(B) two half adder and a NOR gate
(C) two half adder and OR gate
(D) two half adder and AND gate

i. A ring counter consisting of 5 flipflop will have

(A) 5 states
(B) 10 states
(C) 32 states
(D) ∞ states

j. LEDs function like normal diodes except they have a forward voltage drop of approximately _____

(A) 0.3 V
(B) 0.7 V
(C) 1V
(D) 2V

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Find the Butterworth transfer function that meets the following low pass filter specification $f_p = 10KHz$, $A_{max} = 1dB$, dc gain = 1, $A_{min} = 25dB$. **(8)**

b. Explain "offset voltage" and "offset current" of an opamp also discuss the technique for minimizing the same. **(8)**

Q.3 a. Explain the basic principle of switching capacitor filter and also explain how a switching capacitor behave as a resistance. **(6)**

b. Draw the block diagram for a counting type A/D converter and explain the operation for the system. **(10)**

Q.4 a. Explain the physical significance of storage time and transition time in diode switching. **(8)**

b. Explain the terms
(i) Noise margin
(ii) Propagation delay
(iii) Power dissipation
(iv) fan in and fan out **(8)**

Q.5 a. Draw a totem pole output with a TTL gate & explain its operation. **(10)**

b. Generate the following combination logic equation using a 4 input multiplexer $Y = C\,\overline{B}\,\overline{A} + \overline{C}\,\overline{B}\,\overline{A} + C\,\overline{B}\,A + \overline{C}\,B\,A$ **(6)**

Q.6 a. Explain the system for a 4 bit odd parity checker. **(8)**

b. Show how a SR flipflop can be constructed using NOR gates and explain the different states of the SR flipflop. **(8)**

Q.7 a. Explain the block diagram of a ROM and what hardware constitutes the memory element. **(8)**

b. Draw the circuit diagram of a simple instrumentation amplifier. Also derive the expression of output voltage in terms of the input value and circuit resistance. **(8)**

Q.8 a. Sketch the architecture of an NMOS op-amp and list three reasons why this architecture is employed. **(8)**

b. Explain how a PLA can be used to realize a logical expression. **(8)**

Q.9 Write short note on any **TWO** of the following: **(8×2)**

(i) BJT inverter
(ii) Dynamic MOS
(iii) Shift register
(iv) Programmable Array logic