AMIETE – CS (OLD SCHEME)

Code: AC23   **Subject: MICROPROCESSOR BASED SYSTEM DESIGN**

Time: 3 Hours   **Max. Marks: 100**

JUNE 2011

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1   **Choose the correct or the best alternative in the following:**   **(2×10)**

a. A certain SRAM has $\overline{CS} = 0$, $\overline{WE} = 0$ and $\overline{OE} = 1$. In which of the following modes this SRAM is operating

   (A) Read   **(B)** Write
   (C) Stand by   **(D)** None of the above

b. What will be the contents of register AL after the following has been executed
   MOV BL, 8C
   MOV AL, 7E
   ADD AL, BL

   (A) 0A and carry flag is set   **(B)** 0A and carry flag is reset
   (C) 6A and carry flag is set   **(D)** 6A and carry flag is reset

c. Ready pin of a microprocessor is used

   (A) To indicate that the microprocessor is ready to receive inputs.
   (B) To indicate that the microprocessor is ready to receive outputs.
   (C) To introduce wait states.
   (D) To provide direct memory access.

d. Signal voltage ranges for a logic high and for a logic low in RS-232C standard are

   (A) Low =0 volt to 1.8 volt, high = 2.0 volt to 5 volt
   (B) Low =-15 volt to –3 volt, high = +3 volt to +15 volt
   (C) Low =+3 volt to +15 volt, high = -3 volt to -15 volt
   (D) Low = 2 volt to 5.0 volt, high = 0 volt to 1.8 volt

e. The PCI bus is the important bus found in all the new Pentium systems because

   (A) It has plug and play characteristics
   (B) It has ability to function with a 64 bit data bus
   (C) Any Microprocessor can be interfaced to it with PCI controller or bridge
   (D) All of the above

f. The 8088 microprocessor has

   (A) 16 bit data bus   **(B)** 4 byte pre-fetch queue
   (C) 6 byte pre-fetch queue   **(D)** 16 bit address bus

g. If the crystal oscillator is operating at 15 MHz, the PCLK output of 8284 is

   (A) 2.5 MHz   **(B)** 5 MHz
   (C) 7.5 MHz   **(D)** 10 MHz

h. Which type of JMP instruction assembles, if the distance is 0020 h bytes?

   (A) near   **(B)** far
   (C) short   **(D)** none of the above

i. By what factor does the 8284A clock generator divide the crystal oscillator's output frequency?

   (A) One   **(B)** Two
   (C) Three   **(D)** Four

j. When the 82C55 is reset, its I/O ports are all initializes as

   (A) output port using mode 0   **(B)** Input port using mode 1
   (C) output port using mode 1   **(D)** Input port using mode 0

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What do you mean by BIOS call? **(4)**

   b. What do you understand by addressing mode? Discuss briefly various addressing mode. **(12)**

Q.3 a. Interfaced 2k × 8 (i.e 2716) EPROM using multiple input NAND gate decoder for memory locations FF800H-FFFFFH. **(6)**

   b. What is TPA (transient program area)? Draw the memory map of TPA in a personal computer and explain different areas. **(5)**

   c. What is memory paging? Explain how it is used for memory addressing. **(5)**

Q.4 a. Describe in detail the hardware interrupts available in INTEL family. **(8)**

b. Write a Program in assembly language to find the largest of n numbers stored in the memory. **(8)**

Q.5 a. Explain in detail the operation of 8255 in mode1 taking suitable example. **(10)**

b. Give various modes of operation of 8254. **(6)**

Q.6 a. Draw and explain the basic architecture of 80186. **(10)**

b. Discuss briefly MMX technology and its instruction set. **(6)**

Q.7 a. Explain the following instructions:

(i) TEST (ii) NEG (iii) CMP (iv) DAA (v) PUSH (vi) POP **(8)**

b. Write short note on Assembler directives. **(8)**

Q.8 Write short notes on:- **(4×4)**

(i) RTOS
(ii) Real time clock
(iii) Protected and virtual mode of 8086
(iv) Super scalar architecture.

Q.9 a. Explain the operation of 8279. Also explain the following terms: **(6)**

(i) N key Roll over
(ii) Key board debounce
(iii) FIFO RAM.

b. What do you mean by A/D conversion? Explain any one of the following A/D techniques: **(10)**

(i) Successive approximation. (ii) Parallel / flash converter.