ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **December - 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which one of the following is **NOT** a process step in CMOS technology?
(A) n+ active area **(B)** active p+ area
(C) gate oxidation **(D)** n+ buried layer

b. Given that hole mobility is $50cm^2/V\text{-}s$, K is $2\times 10^{-3}AV^{-2}$, width to channel length ratio is 10. The source to drain voltage is 2.5 V. When a pMOS transistor just enters saturation, the measured value of source to drain current is 40mA. The value of threshold voltage is _____.
(A) 0.4 V **(B)** -0.4 V
(C) 0.25 V **(D)** -0.25 V

c. Design rule violation results in
(A) yield loss **(B)** reliability issues
(C) fabrication difficulties **(D)** All of these

d. A piece of wire is 4 units long 1 unit wide. If the thickness of wire is 0.5μm and resistivity is 10 Ωcm, then the resistance of wire is _____ Ω.
(A) 1.25 **(B)** 0.8
(C) 80 **(D)** 0.0125

e. Switch logic is based on
(A) pass transistor **(B)** transfer transistor
(C) latch transistor **(D)** nMOS logic

f. Partitioning of system facilitates
(A) reduces complexity **(B)** reduces timing
(C) reduces area of circuit **(D)** All of these

g. The biggest problem of dynamic logic is
(A) unequal noise margin **(B)** cascading
(C) high output capacitance **(D)** high leakage power

h. The regularity of a 4 × 4 barrel shifter is _____.
(A) 4 **(B)**16
(C) 32 **(D)** 2

i. In a given technology node, the area of a CMOS inverter depends on
(A) carrier mobility **(B)** channel length
(C) current driving capability **(D)** supply voltage

j. Which one of the following is a design related issue?
(A) dielectric breakdown **(B)** via open
(C) electromigration **(D)** All of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Compare CMOS and bipolar technologies. **(6)**

b. Summarize typical processing steps involved in pMOS fabrication process. **(8)**

c. Why depletion mode MOSFET is not preferred in CMOS design? **(2)**

Q.3 a. Explain the frequency figure of merit of a MOS transistor. **(4)**

b. Explain working of an nMOS inverter and draw its voltage transfer characteristics. **(6)**

c. Determine the pull-up to pull-down ratio of an nMOS inverter driven by another nMOS inverter. **(6)**

Q.4 a. Draw stick diagram of a p-well CMOS inverter. **(6)**

b. Draw stick diagram of nMOS two input NOR gate and CMOS two input NOR gate. **(10)**

Q.5 a. Why silicides are required? How silicides are processed? **(4)**

b. Find an expression for rise time of a symmetric inverter. If a symmetric CMOS inverter drives a load equal to that of ten symmetric inverters, find the rise time if oxide thickness is 10nm, $|V_{TP}|=V_{TN}=0.4V$, $V_{DD}= 1.8V$, $W_n=L_n=180nm$, electron and hole mobility are $150cm^2/V\text{-}s$ and $100cm^2/V\text{-}s$ respectively. **(12)**

Q.6 When a MOSFET is scaled down by combined voltage and dimension scaling, how the following device parameters change? **(16)**

Gate area, Gate delay, saturation current, power dissipation per gate, switching energy per gate, Power speed product, conductor cross section area and supply voltage

Q.7 Explain general steps in VLSI design process. **(16)**

Q.8 List various system timing considerations. **(16)**

Q.9 Explain Design styles and Philosophy. **(16)**